

BAD50 HR

DIS/UMA/Muxless Schematics Document

Sandy Bridge

Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

D12G

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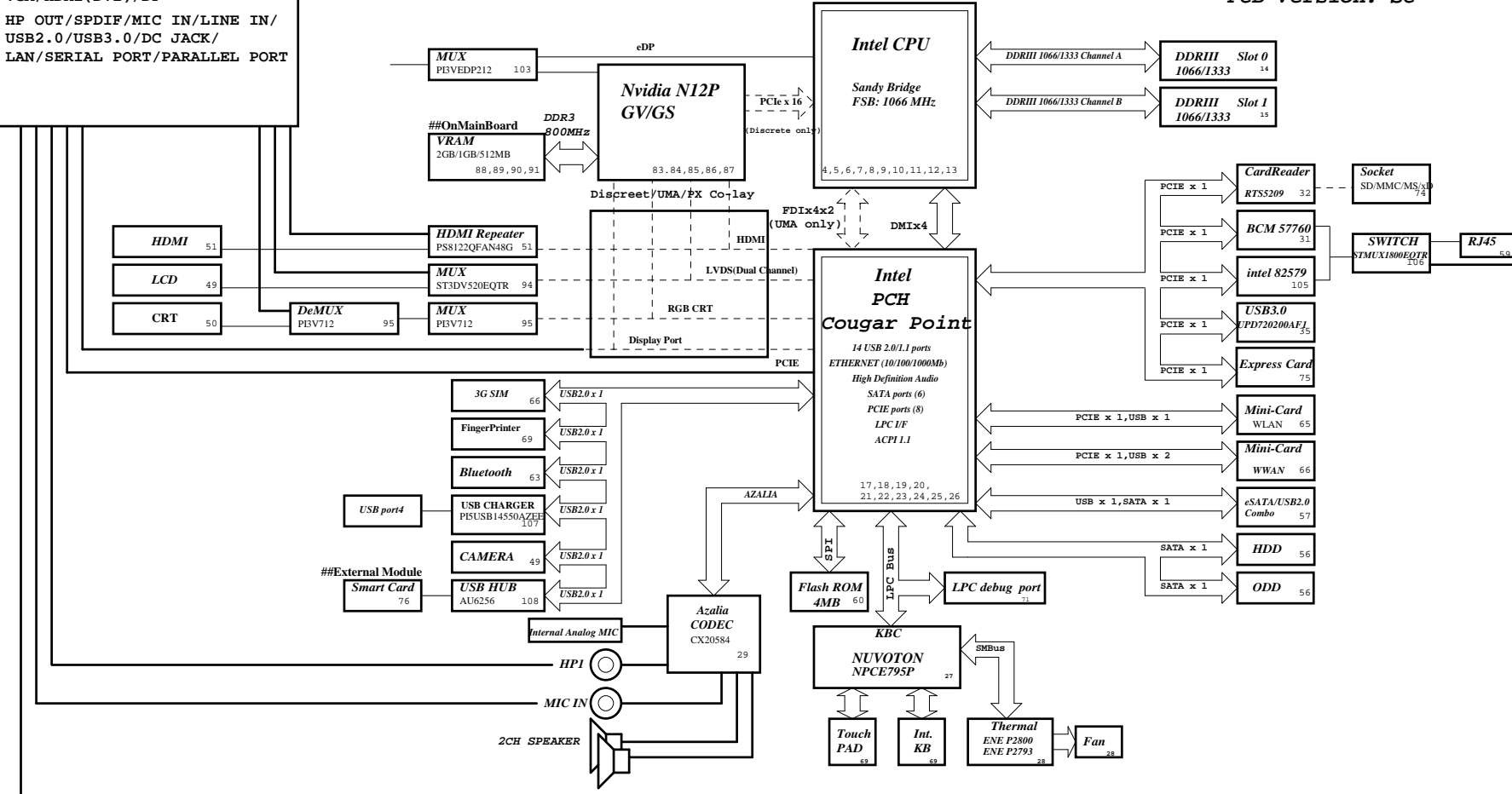
File		
Cover Page		
Size A3	Document Number BA40/50-HR	Rev SD
Date: Thursday, April 07, 2011	Sheet 1	of 109

BAD50-HR Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4NM01.001
Project Name: BAD50_HR
PCB No: 10309
PCB Version: SC

Buttom Docking

VGA/HDMI (DVI) /DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT



SYSTEM DC/DC	
TPS5146	48
INPUTS	OUTPUTS
5V_S5	0D85V_S0
CPU DC/DC	
VT1317SFCX	42-43
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
RT8237AGQW	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8237CGQW	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC	
RT8207LGQW	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 VDD_VREF_S3
SYSTEM DC/DC	
VT1317SFCX	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR
VGA	
RT8208AGQW	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
TI CHARGER	
BQ24745RHDR	40
INPUTS	OUTPUTS
DCBATOUT	ST+
SYSTEM DC/DC	
RT8015AGQW	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
SYSTEM DC/DC	
INPUTS	OUTPUTS
Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0
PCB LAYER	
L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

D126

SSID = CPU

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

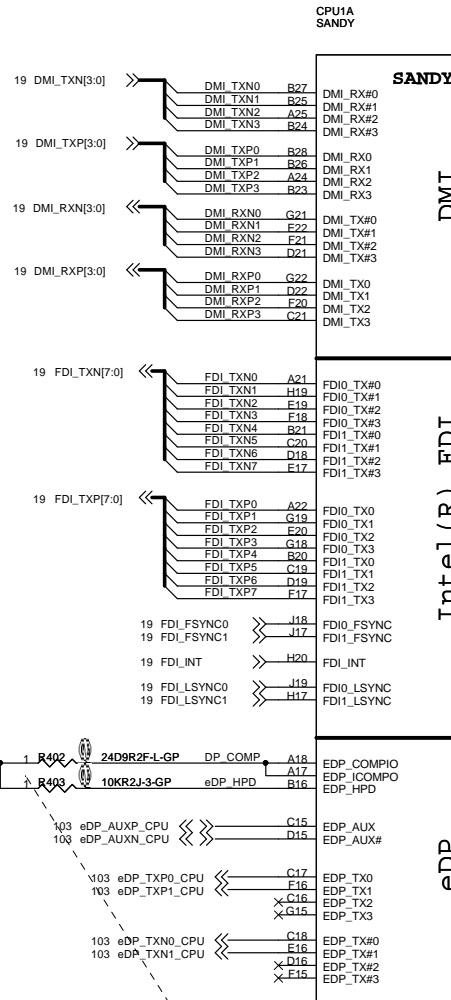
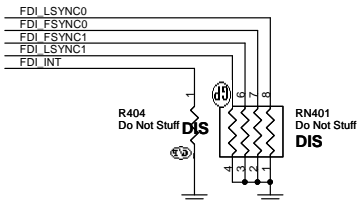
Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

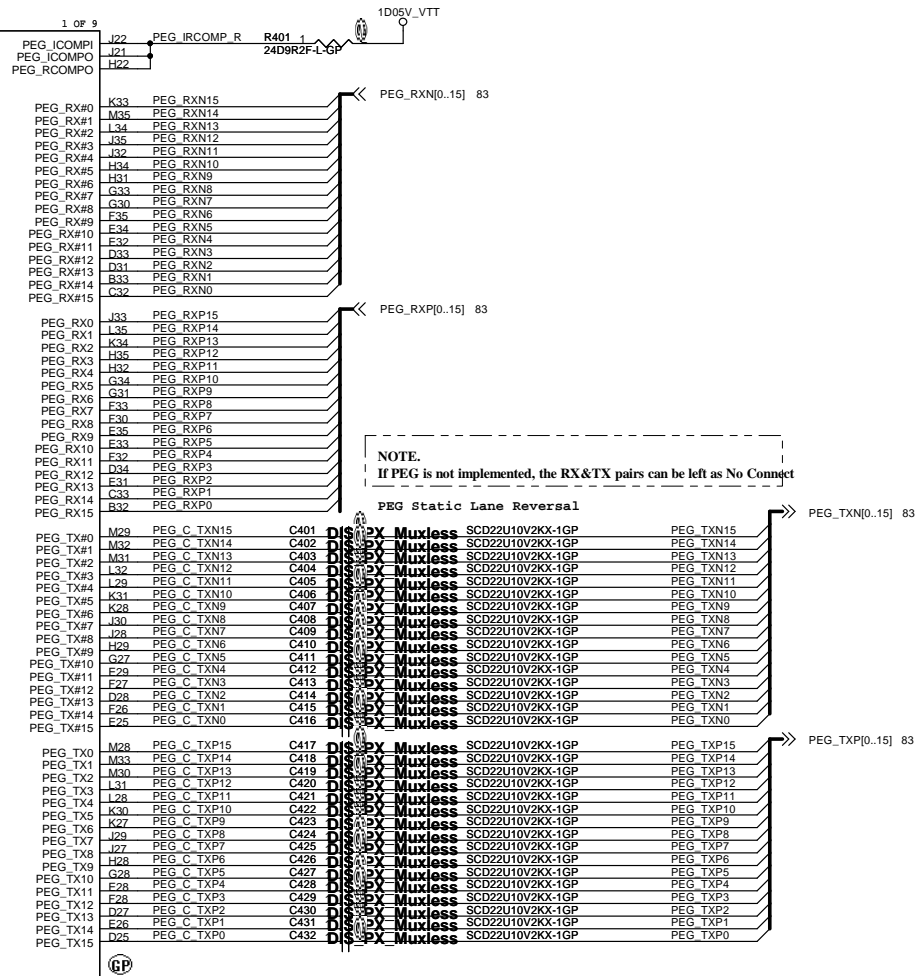
NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics
function for power saving.



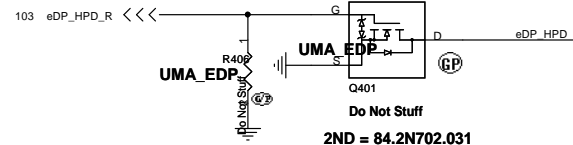
NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



全改MUX

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-k Ω pull-up resistor on the motherboard.

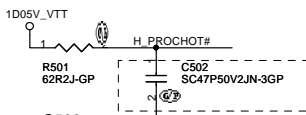


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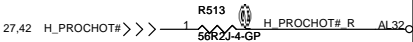
Title			
CPU (PCIe/DMI/FDI)			
Size A3	Document Number		Rev
	BAD50-HR		SD
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SSID = CPU



C502:
47pf@CRB
43pf@CEKLT

Connect EC to PROCHOT# through inverting OD buffer.



18 H_SNB_IVB# <<< C26

JE40 modify

JE40 modify

22,27 H_PECI <<> AN33

27,42 H_PROCHOT# >>> 1 R513 50R2J-4-GP

22,36 H_THERMTRIP# <<< AN32

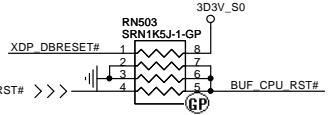
19 H_PM_SYNC <<> AM34

22,36,97 H_CPUPWRGD >>> 1 R503 10K R2J-2-GP

19,37 PM_DRAM_PWRGD >>> 1 R505 10K R2J-2-GP

37 VDDPWRGOOD >>> 1 R505 10K R2J-2-GP

BUF_CPU_RST# AR33



CPU1B
SANDY

SANDY

MISC

THERMAL

PWR MANAGEMENT

MISC

DDR3

JTAG & BPM

2 OF 9

CLK_EXP_P 20

CLK_EXP_N 20

CLK_DP_P_R 20

CLK_DP_N_R 20

SM_DRAMRST# 37

SM_RCOMP_0 R506 1

SM_RCOMP_1 R507 1

SM_RCOMP_2 R508 1

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

AP23

AP24

AP25

AP26

AP27

AP28

AP29

AP30

AP31

AP32

AP33

AP34

AP35

AP36

AP37

AP38

AP39

AP40

AP41

AP42

AP43

AP44

AP45

AP46

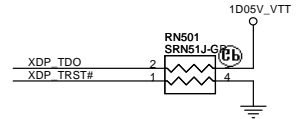
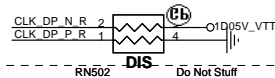
AP47

AP48

AP49

AP50

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistor, power (~15 mW) may be
wasted.



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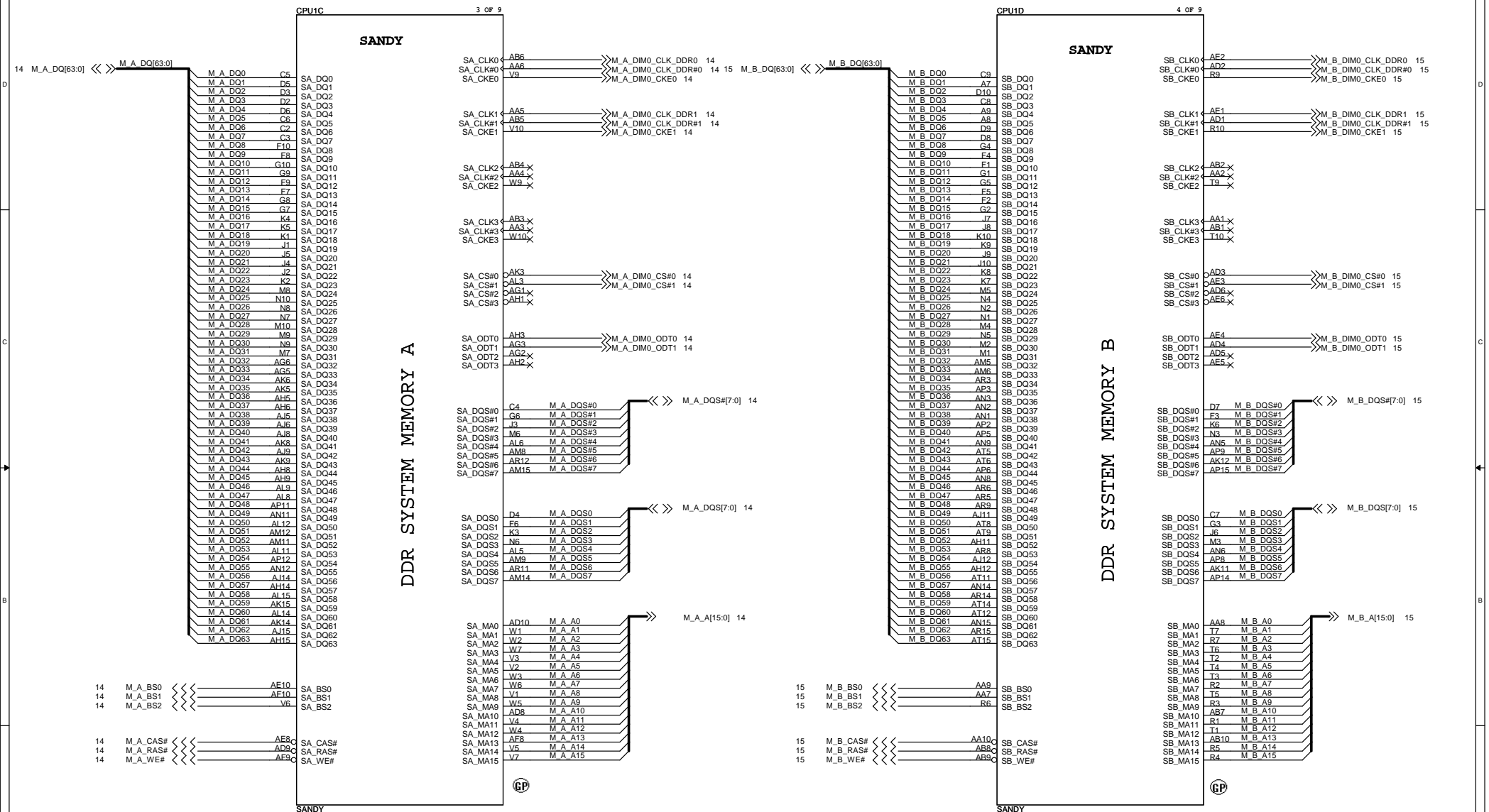
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Title CPU (THERMAL/CLOCK/PM)

Size Custom Document Number BA40-HR Rev SD

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SSID = CPU



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Title

CPU (DDR)

Size

A3

Document Number

BA40-HR

Rev

SD

Date:

Thursday, April 07, 2011

Sheet

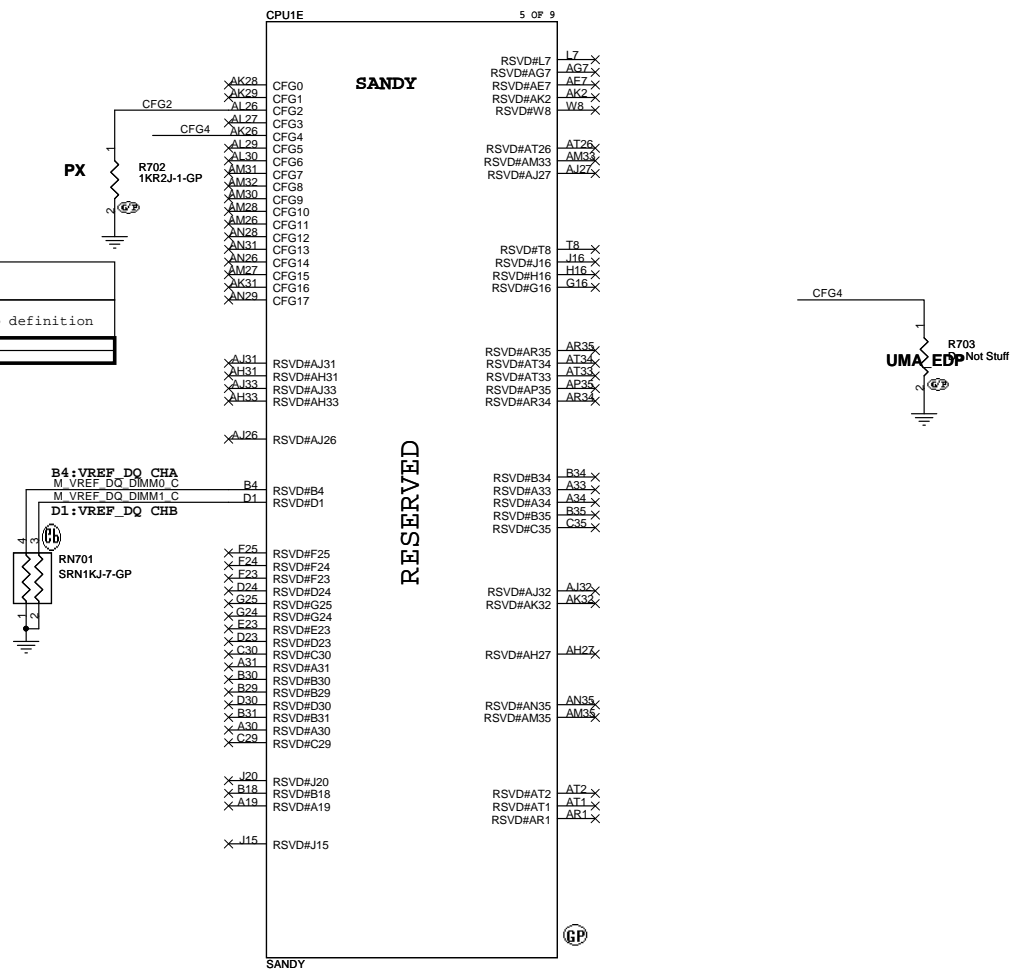
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SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed



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PROCESSOR CORE POWER

53A

SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

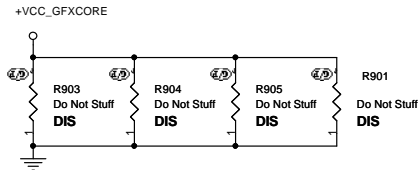
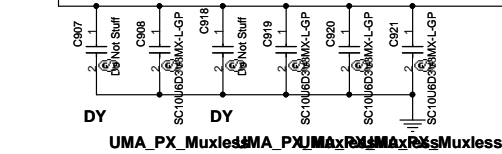
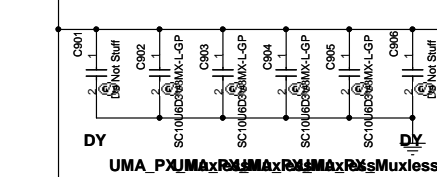
VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

SSID = CPU

VAXG Output Decoupling Recommendation:
 2 x 470 uF at Bottom Socket Edge
 2 x 22 uF at Top Socket Cavity
 4 x 22 uF at Top Socket Edge
 2 x 22 uF at Bottom Socket Cavity
 4 x 22 uF at Bottom Socket Edge

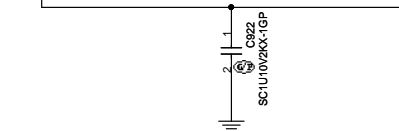
R906, R907 close to CPU

PROCESSOR VAXG: 24A



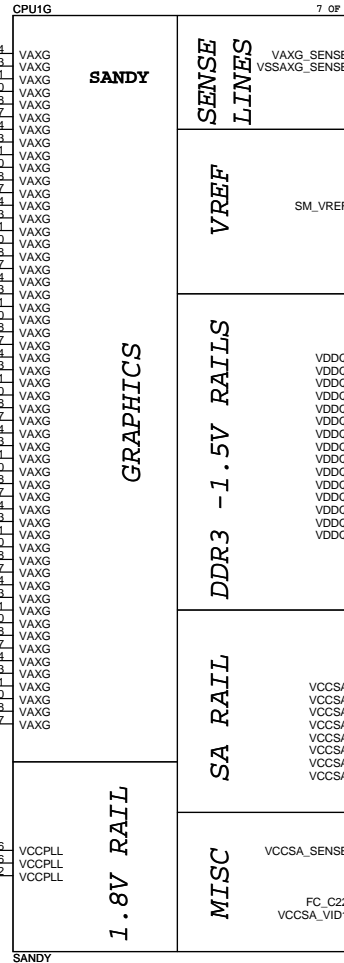
Disabling Guidelines for External Graphics Designs:
 Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
 Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

PROCESSOR VCCPLL: 1.2A



VCCPLL Output Decoupling Recommendation:
 1 x 330 uF
 2 x 1 uF
 1 x 10 uF

POWER

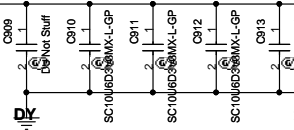


Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

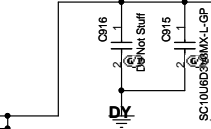
Routing Guideline:
 Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

PROCESSOR VDDQ: 10A



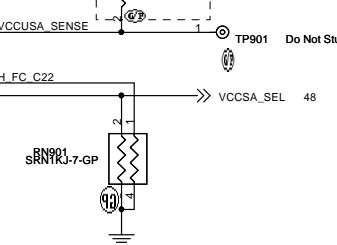
VDDQ Output Decoupling Recommendation:
 1 x 330 uF
 6 x 10 uF

PROCESSOR VCCSA: 6A



VCCSA Output Decoupling Recommendation:
 1 x 330 uF
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge

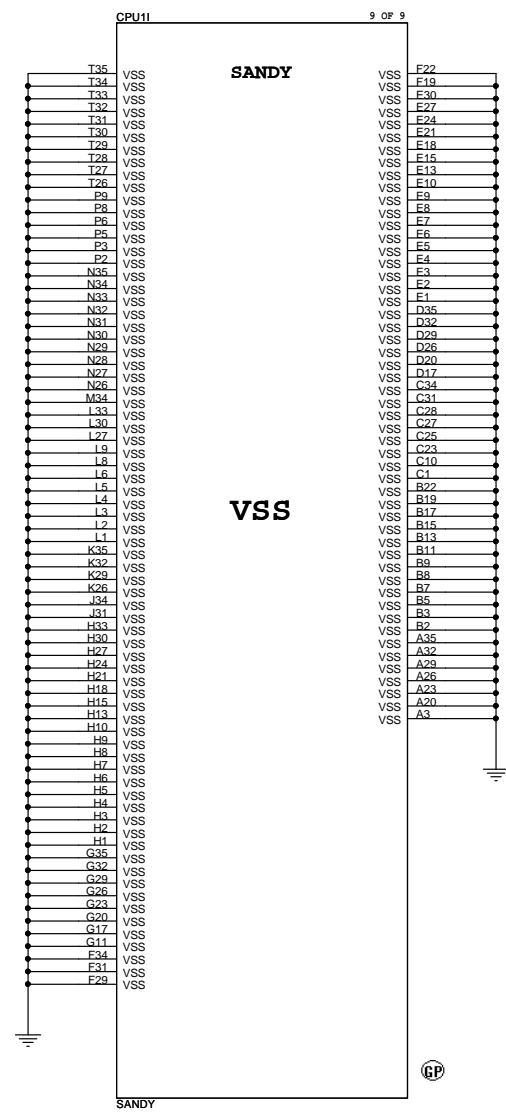
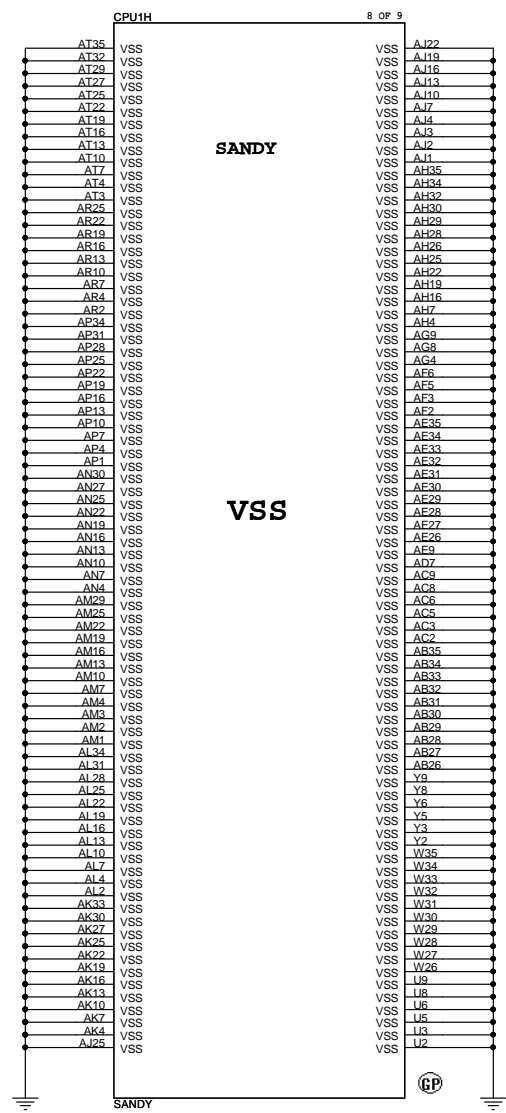
R902 need be close to pin H23.



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SSID = CPU



JE40 delete XDP function

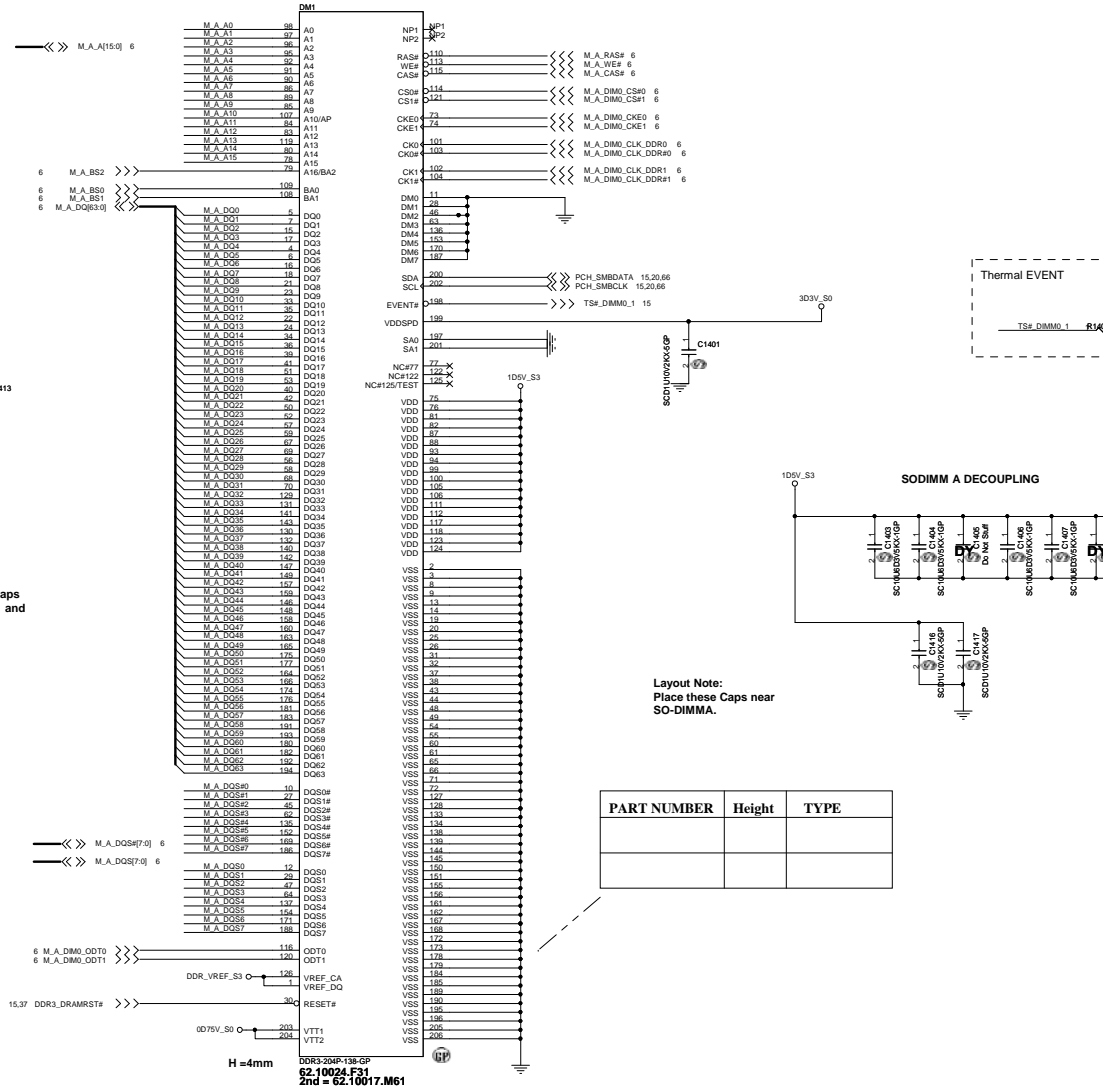
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Title XDP		
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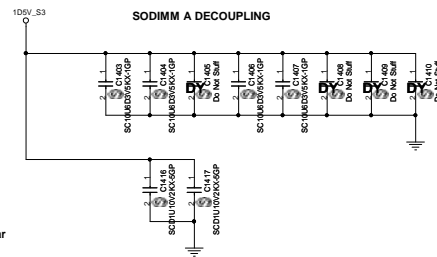
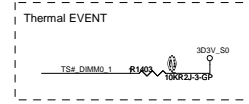
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Title		
Reserved		
Size	Document Number	Rev
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SSID = MEMORY



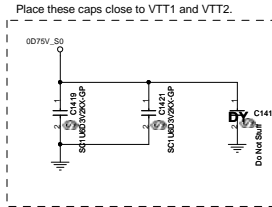
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

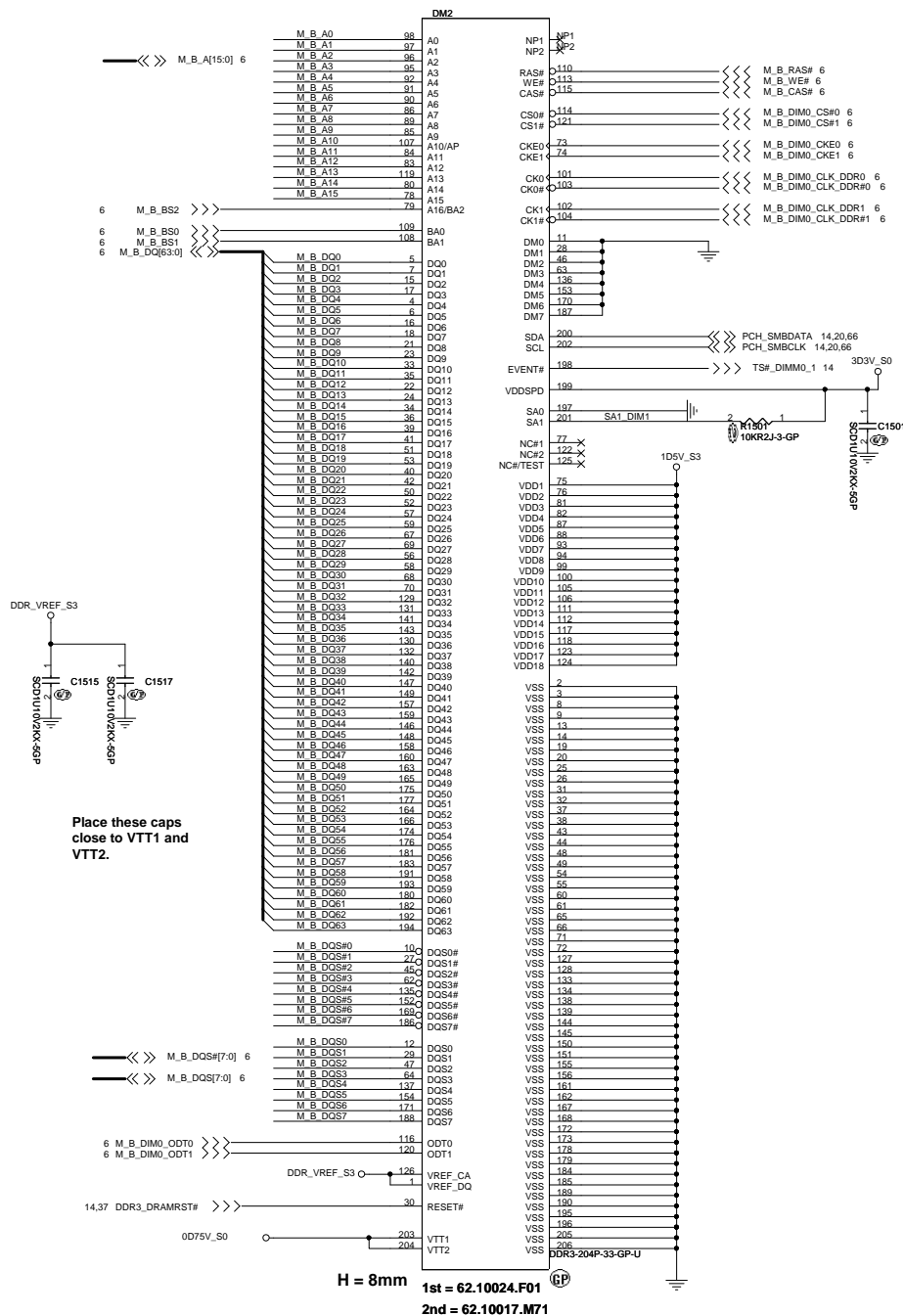


Layout Note:
Place these Caps near
SO-DIMMA.

PART NUMBER	Height	TYPE

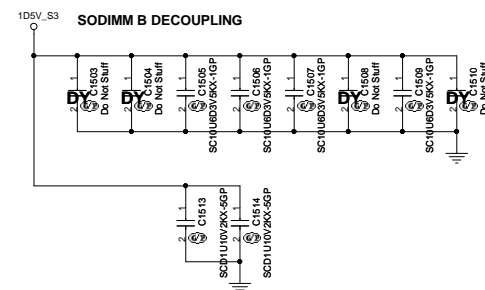
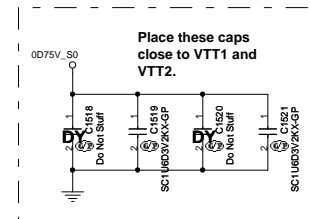


SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near
SO-DIMMB.

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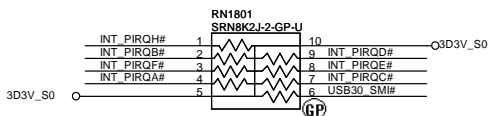
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DDR3-SODIMM2			
Size	Document Number	Rev	
Custom	BA40-HR	SD	
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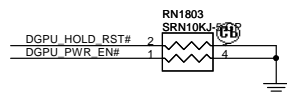
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Title		
DDR3-SODIMM2		
Size	Document Number	Rev
A4	BA40-HR	SD
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SSID = PCH

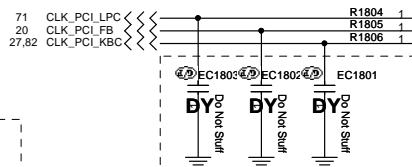
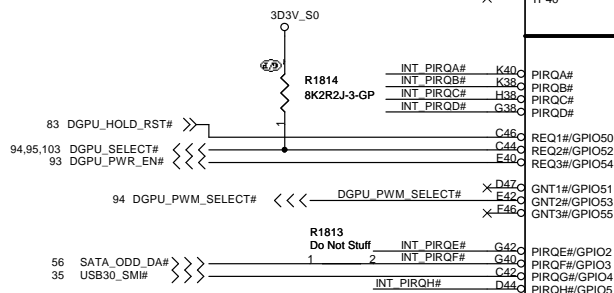


A16 swap override Strap/Top-Block
Swap Override jumper

PCI_GNT#3 Low = A16 swap
override/Top-Block
Swap override enabled
High = Default

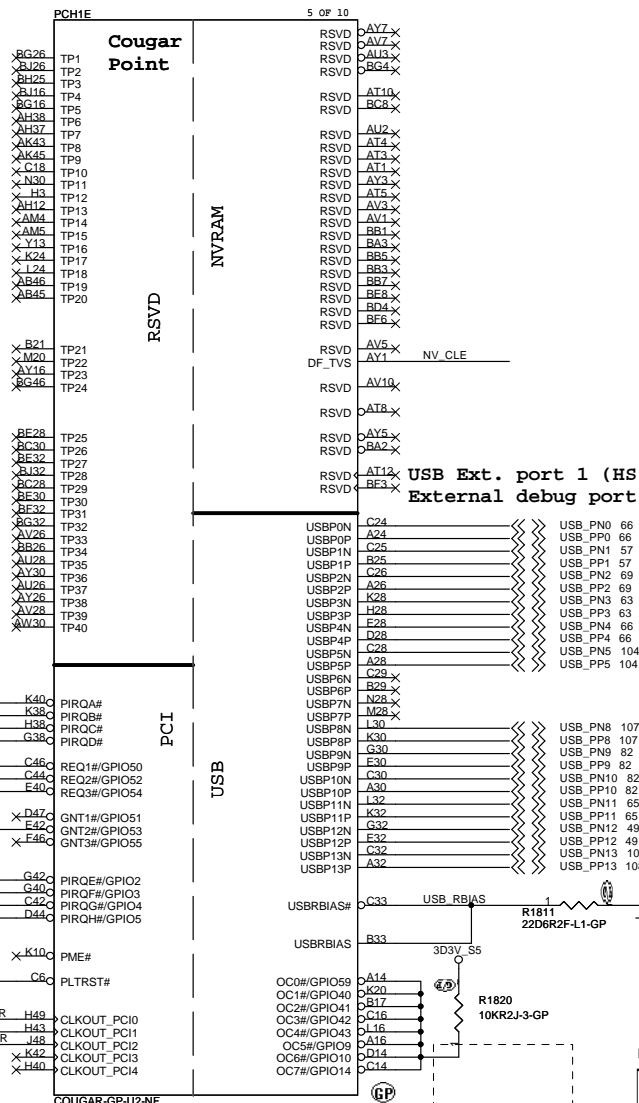


BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



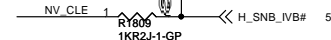
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EMI request 20101109



check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K



DMI & FDI Termination Voltage

NV_CLE	Set to Vss when LOW Set to Vcc when HIGH
--------	---

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	3G Card
1	USB port1(SATA Combo), on M/B
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	Dock
6	X
7	X
8	USB port4 on S/B(usb charger)
9	USB port 2 on S/B
10	USB port 3 (only when 3.0 not support)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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Title			
PCH (PCI/USB/NVRAM)			
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SSID = PCH

4 DMI_RXN[3:0] <<<<
4 DMI_RXP[3:0] <<<<
4 DMI_TXN[3:0] <<<<
4 DMI_TXP[3:0] <<<<

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.

4 DMI_RXN0 <<<< BC24
4 DMI_RXN1 <<<< BE20
4 DMI_RXN2 <<<< BG18
4 DMI_RXN3 <<<< BG20
4 DMI_RXP0 <<<< BE24
4 DMI_RXP1 <<<< BC20
4 DMI_RXP2 <<<< BJ18
4 DMI_RXP3 <<<< BJ20
4 DMI_TXN0 <<<< AW24
4 DMI_TXN1 <<<< AW20
4 DMI_TXN2 <<<< BB18
4 DMI_TXN3 <<<< AV18
4 DMI_TXP0 <<<< AY24
4 DMI_TXP1 <<<< AY20
4 DMI_TXP2 <<<< AY18
4 DMI_TXP3 <<<< AU18

PCH1C

Cougar
Point

DMI

System Power Management

3 OF 10

FDI
BJ14 FDI_RXN0 <<<< FDI_TXN0 4
AY14 FDI_RXN1 <<<< FDI_TXN1 4
BE14 FDI_RXN2 <<<< FDI_TXN2 4
BH13 FDI_RXN3 <<<< FDI_TXN3 4
BC12 FDI_RXN4 <<<< FDI_TXN4 4
BJ12 FDI_RXN5 <<<< FDI_TXN5 4
BG10 FDI_RXN6 <<<< FDI_TXN6 4
BG9 FDI_RXN7 <<<< FDI_TXN7 4
BC14 FDI_RXP0 <<<< FDI_TXP0 4
BB14 FDI_RXP1 <<<< FDI_TXP1 4
BE14 FDI_RXP2 <<<< FDI_TXP2 4
BG13 FDI_RXP3 <<<< FDI_TXP3 4
BE12 FDI_RXP4 <<<< FDI_TXP4 4
BG12 FDI_RXP5 <<<< FDI_TXP5 4
BH10 FDI_RXP6 <<<< FDI_TXP6 4
BH9 FDI_RXP7 <<<< FDI_TXP7 4
AW16 FDI_INT <<<< FDI_INT 4
AV12 FDI_FSYNC0 <<<< FDI_FSYNC0 4
BC10 FDI_FSYNC1 <<<< FDI_FSYNC1 4
AV14 FDI_LSYNC0 <<<< FDI_LSYNC0 4
BB10 FDI_LSYNC1 <<<< FDI_LSYNC1 4

DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

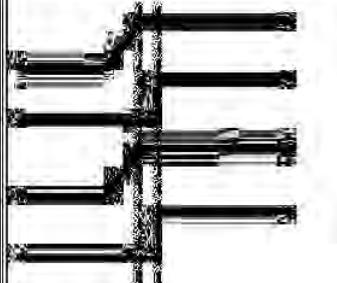
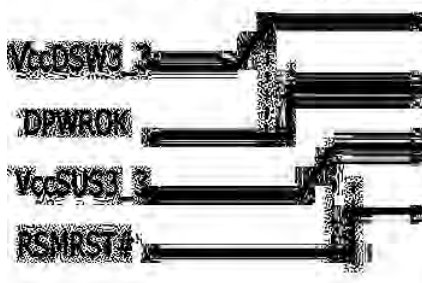
DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

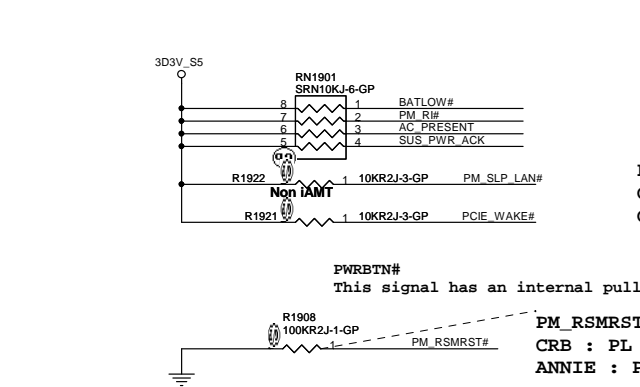
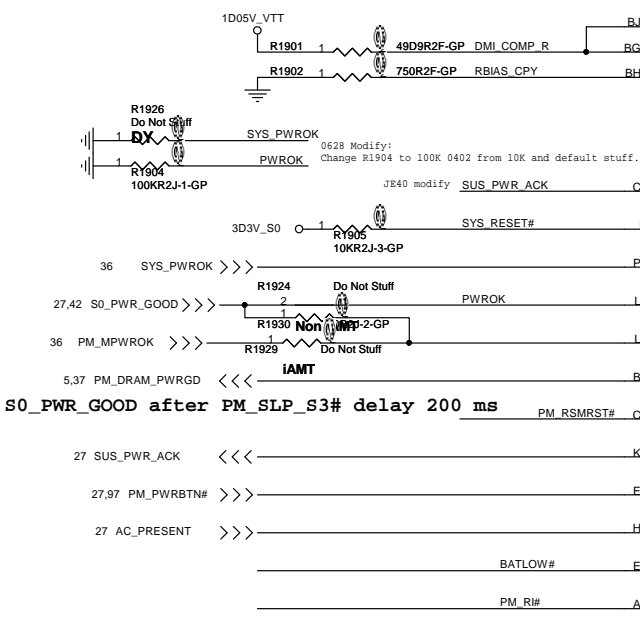
DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK#/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29

Deep S4/S5 Supported

Deep S4/S5 Not Supported

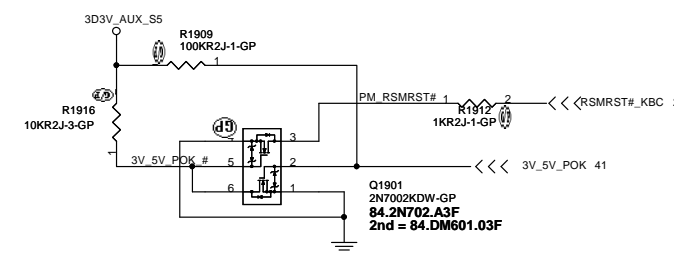


For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWDRNACK/GPIO30

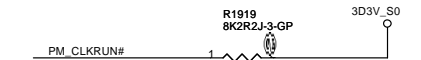


PCIE_WAKE#
CRB : 1K
CEKLT: 10K

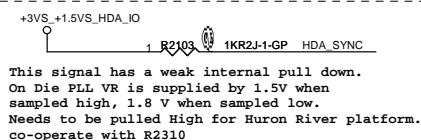
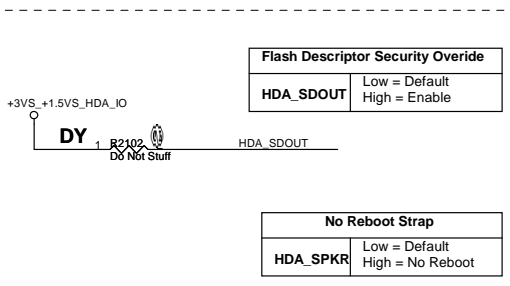
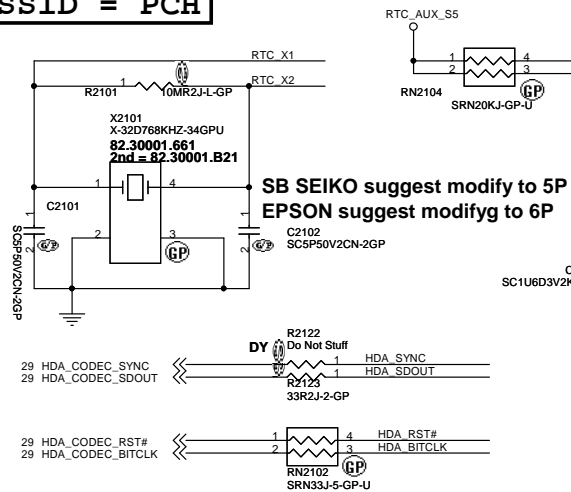
PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K



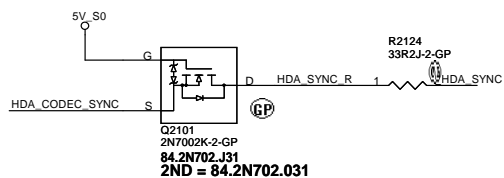
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



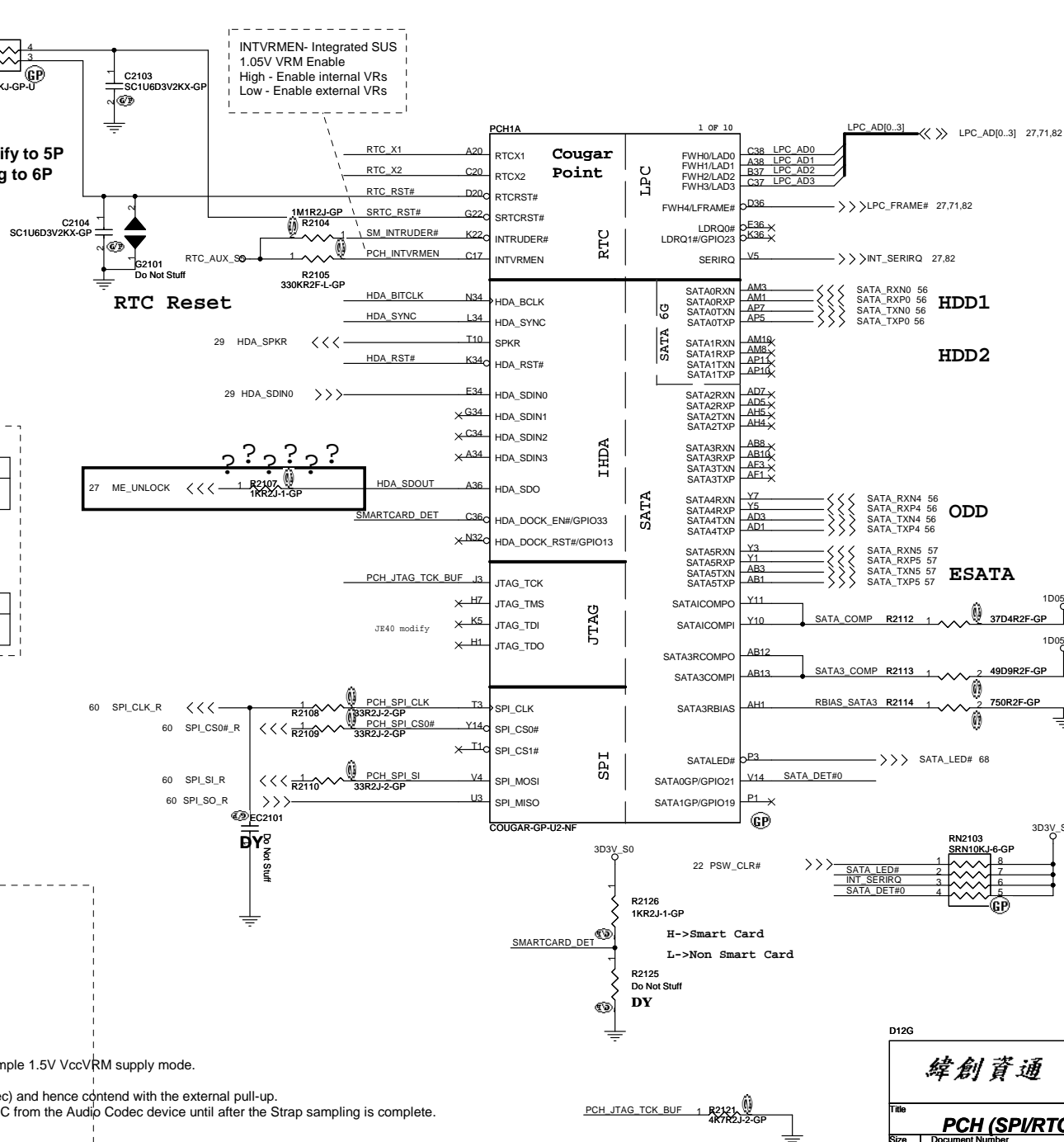
SSID = PCH



PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

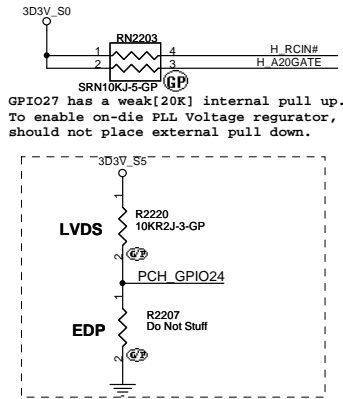


HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode.
1K external pull-up resistor is required on this signal on the board.
Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up.
A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

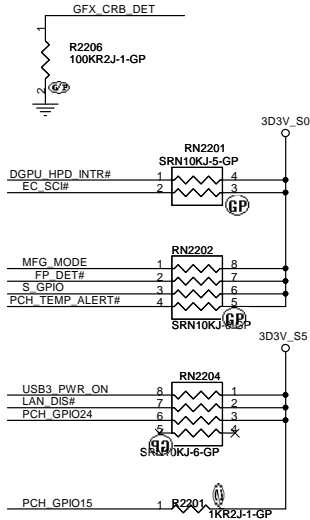


SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

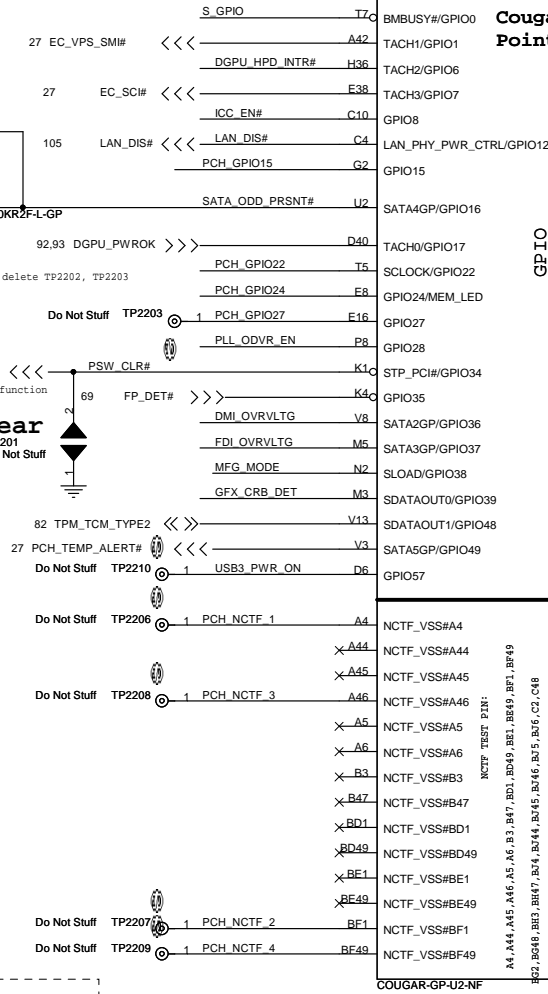
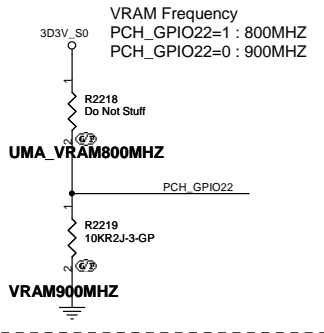
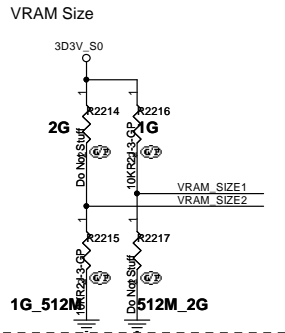


	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

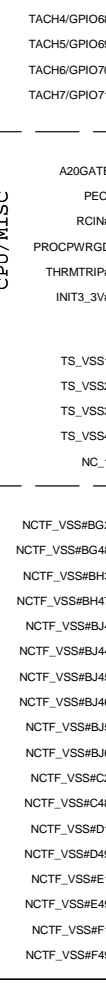


PassWord Clear

G2201
Do Not Stuff



Cougar Point



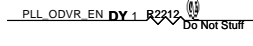
NCTF

NCTF TEST PIN:

A4, A44, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BD2, BD48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, C2, C48, D1, D49, E1, E49, F1, F49

PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)



SB 公板 check different, check need modify or not

Intel R2204

TS Signal Disable Guideline:

TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

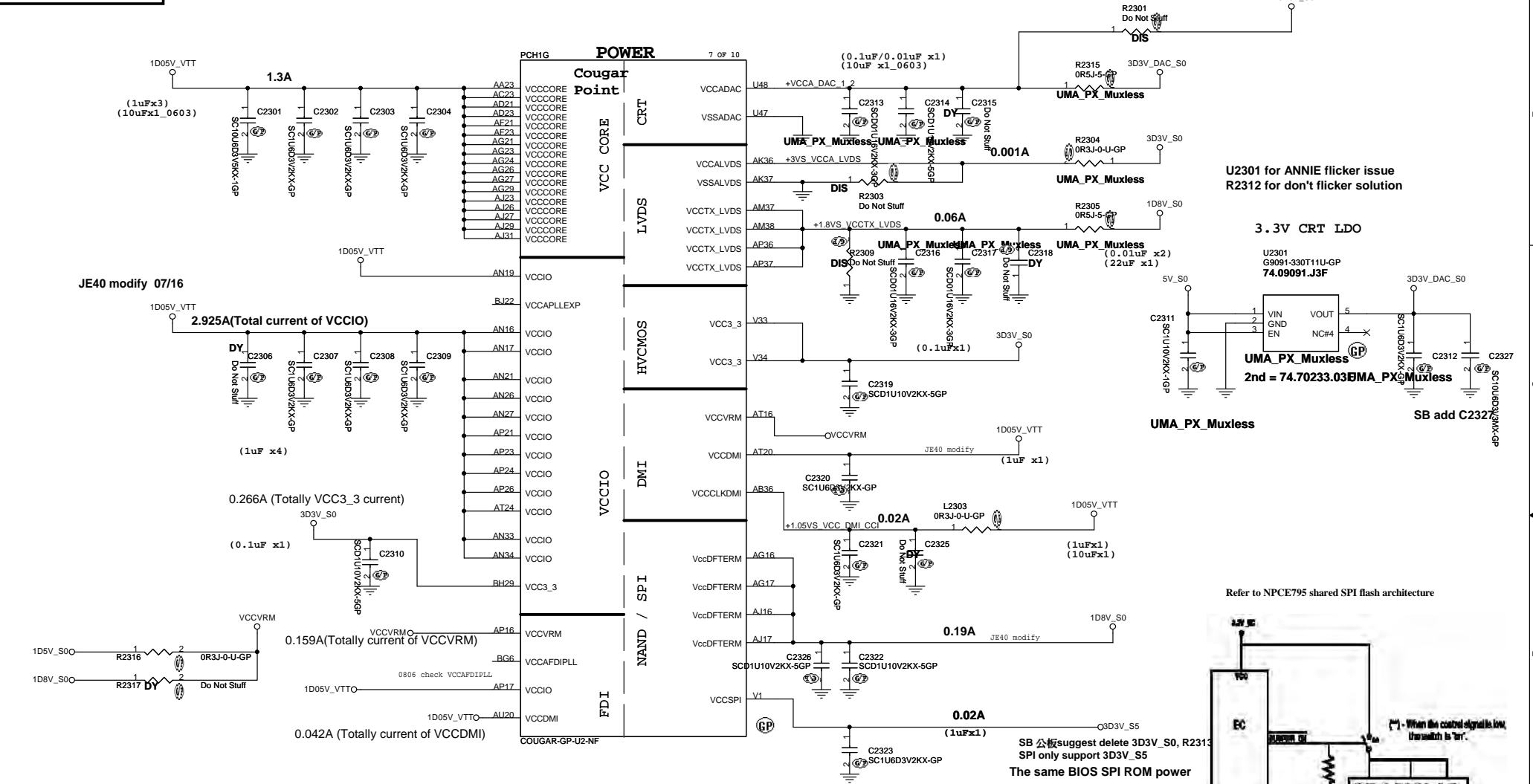
Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up. Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

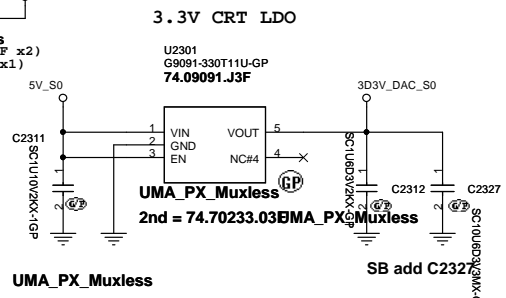
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

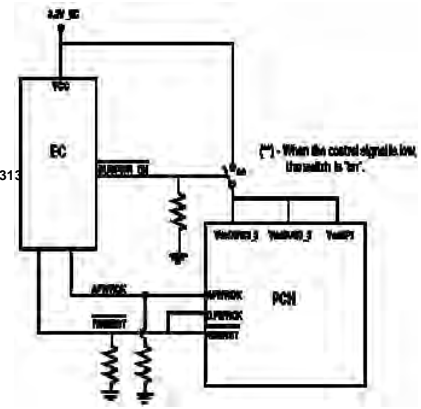
Title		PCH (GPIO/CPU)	
Size A3	Document Number	BA40-HR	
Date: Thursday, April 07, 2011	Sheet	22	of 109

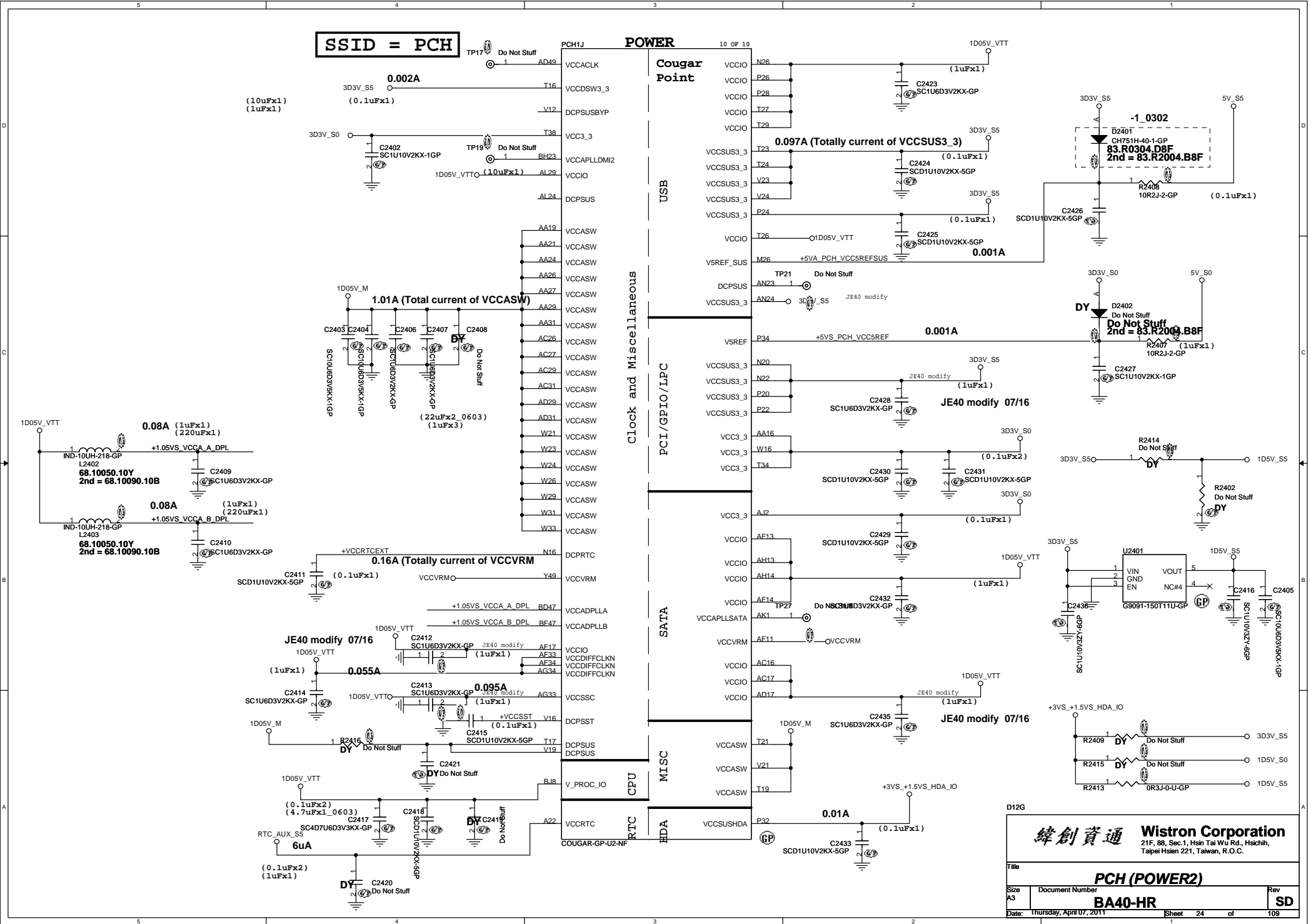


U2301 for ANNIE flicker issue
R2312 for don't flicker solution

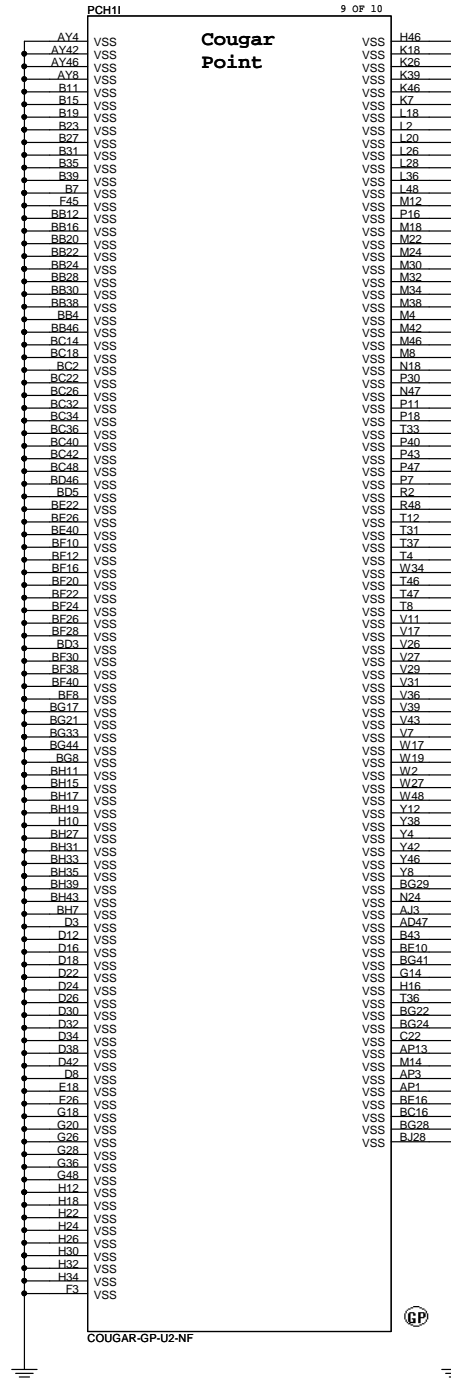
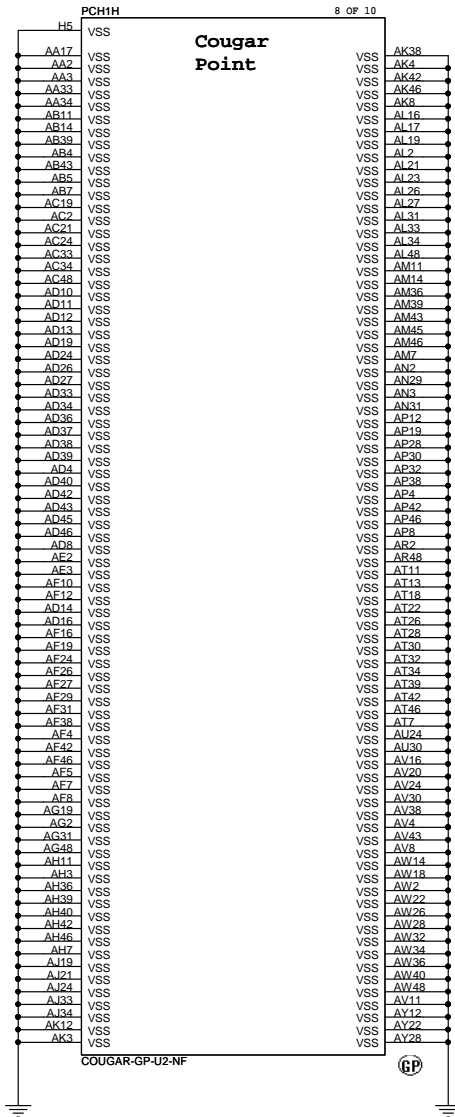


Refer to NPCE795 shared SPI flash architecture





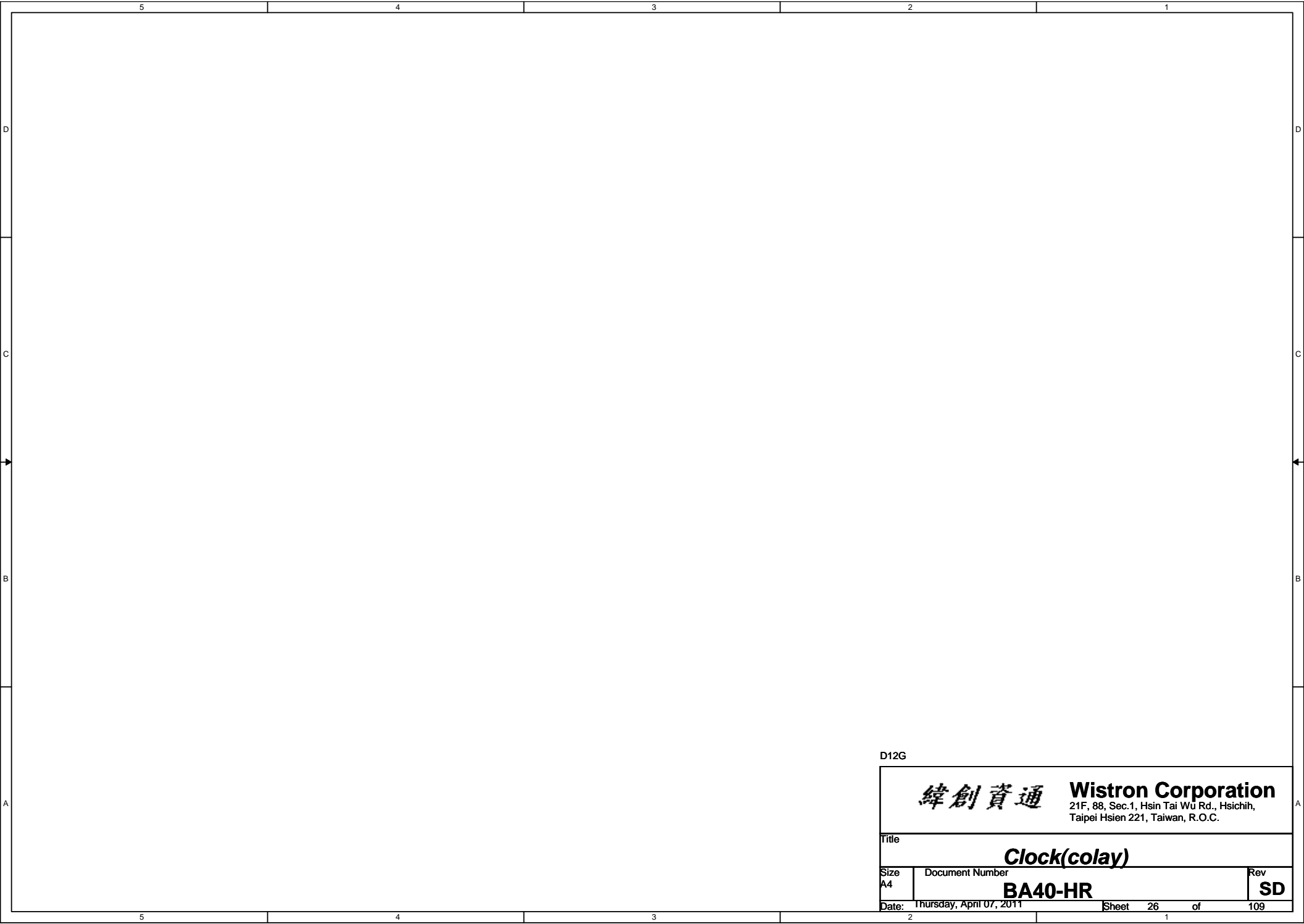
SSID = PCH



D12G

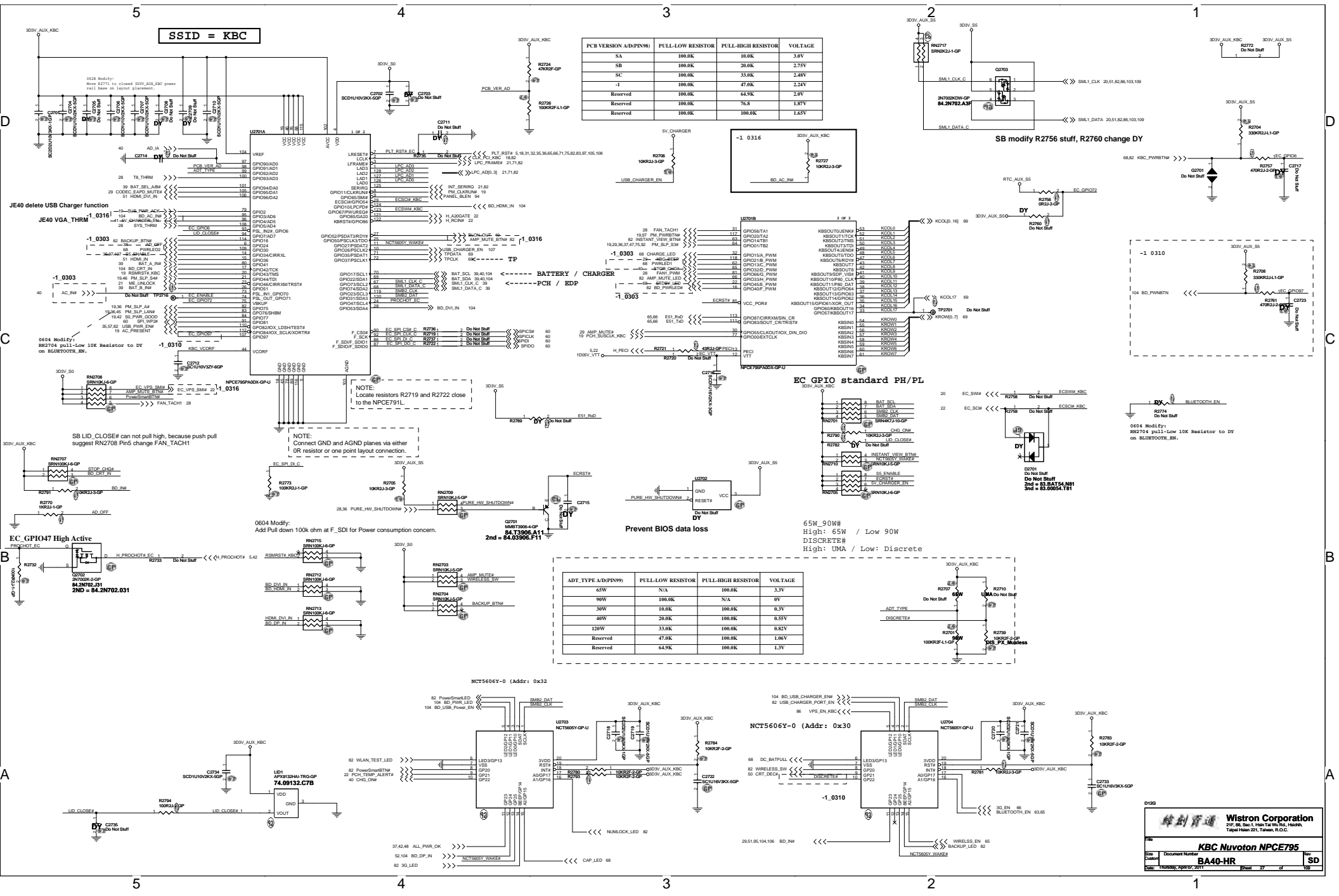
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
PCH (VSS)				
Size A3	Document Number BA40-HR			Rev SD
Date: Thursday, April 07, 2011	Sheet 25		of 109	

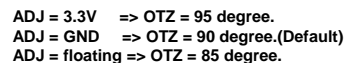
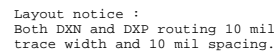


D12G

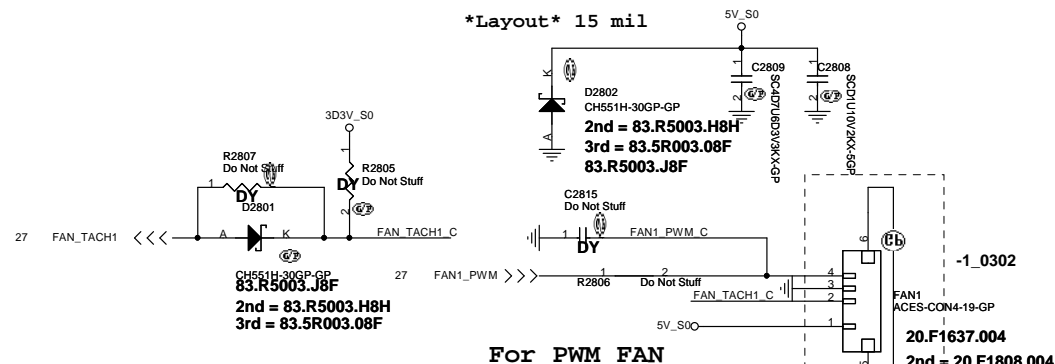
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title <div>Clock(colay)</div>	
Size <div>A4</div>	Document Number <div>BA40-HR</div>
Date <div>Thursday, April 07, 2011</div>	Rev <div>SD</div>
Sheet 26 of 109	



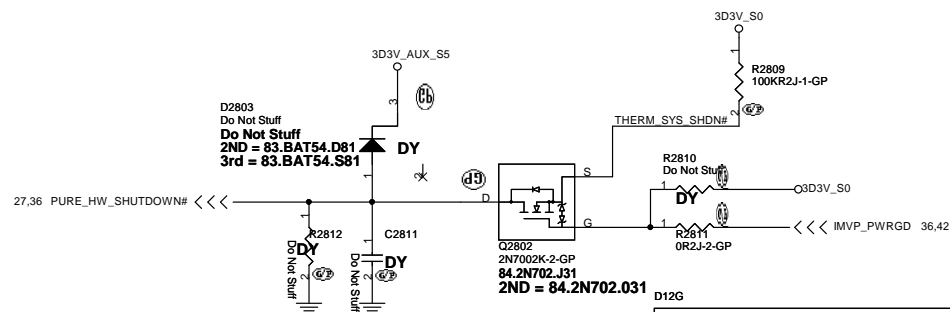
Thermal sensor P2800



-1 0304



For PWM FAN

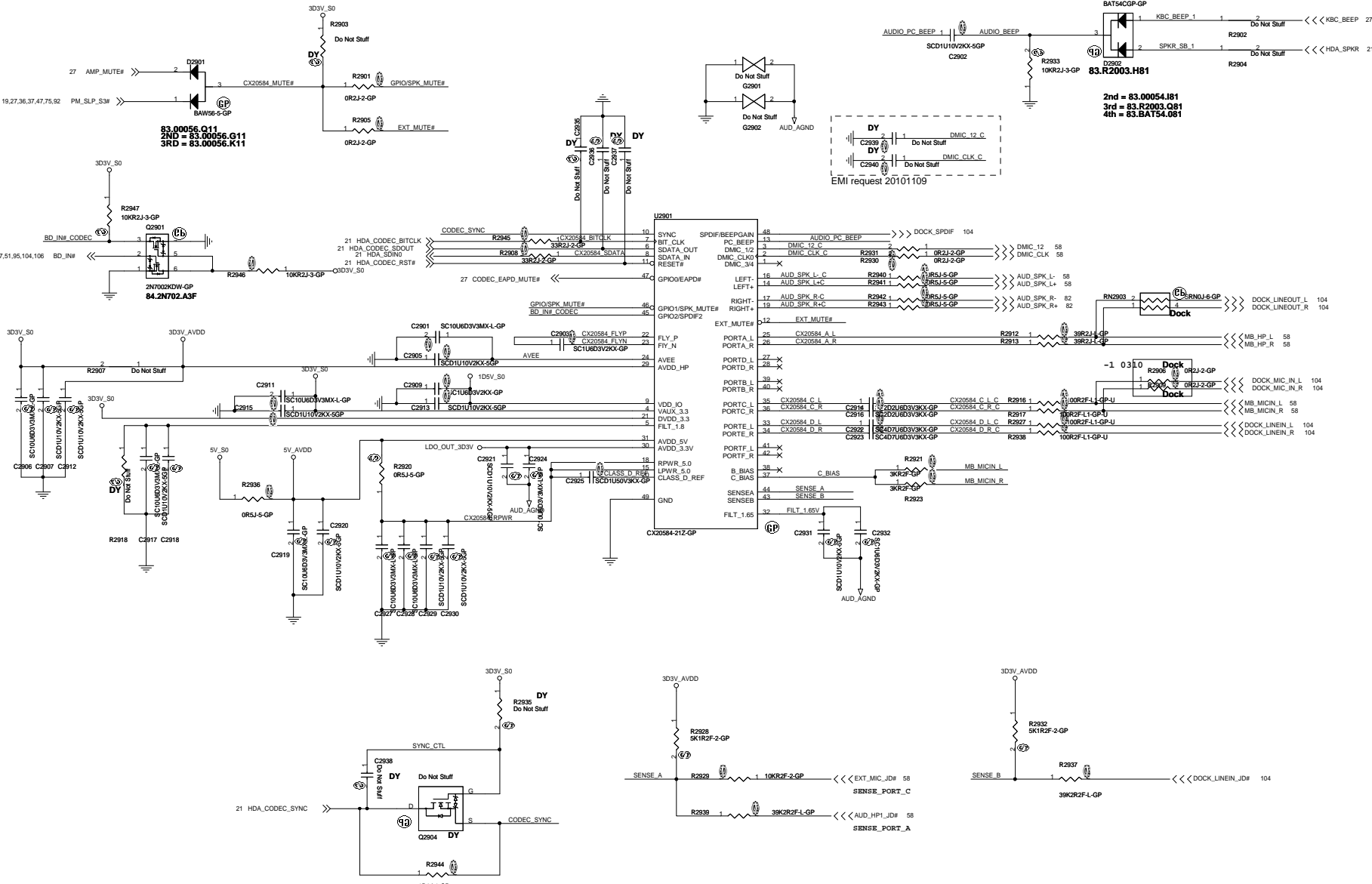


緯創資通

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Title
Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
Custom	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 28 of 109

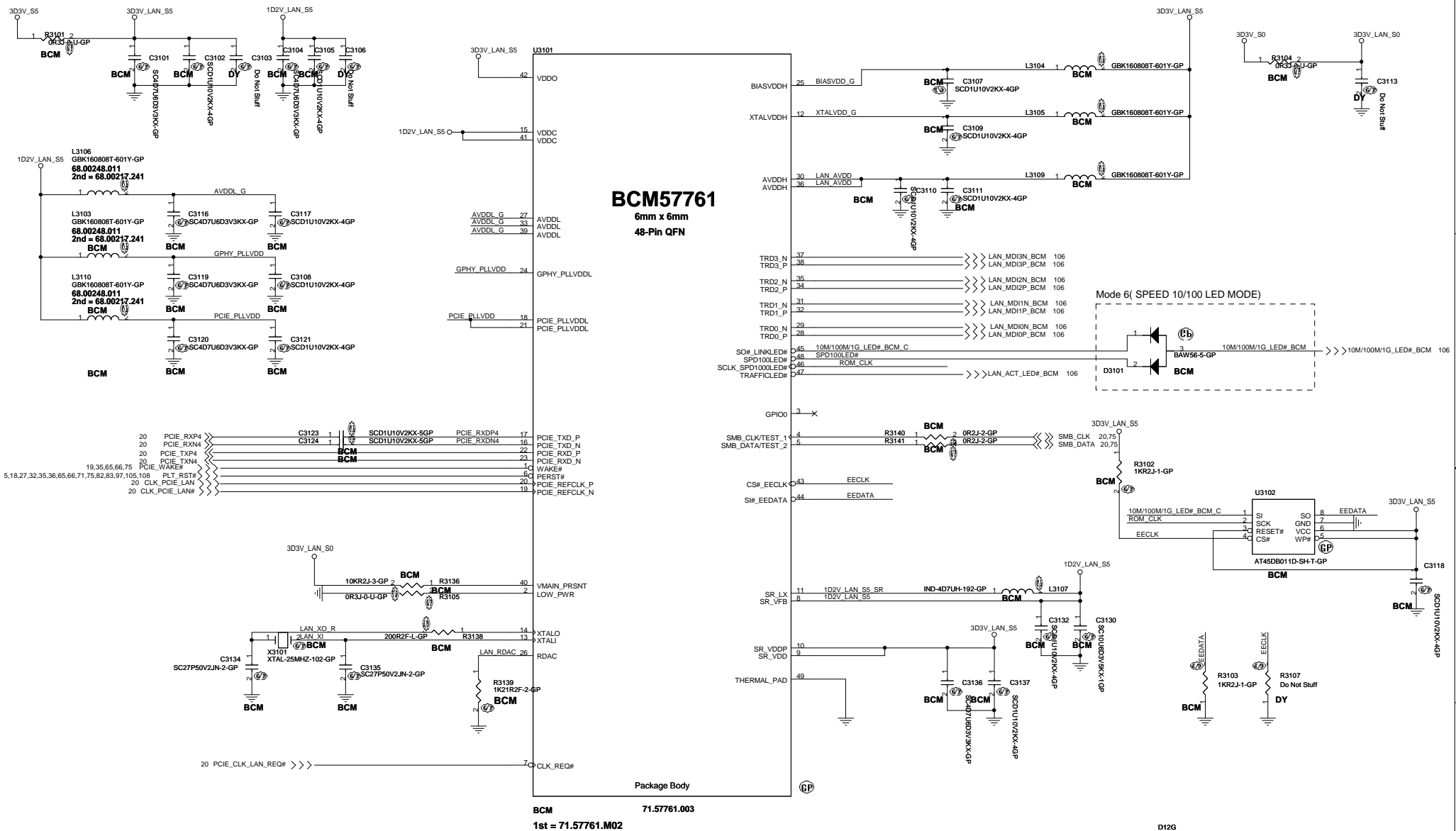


AUDIO OP AMPLIFIER

JE40 delete AMP function

D12G

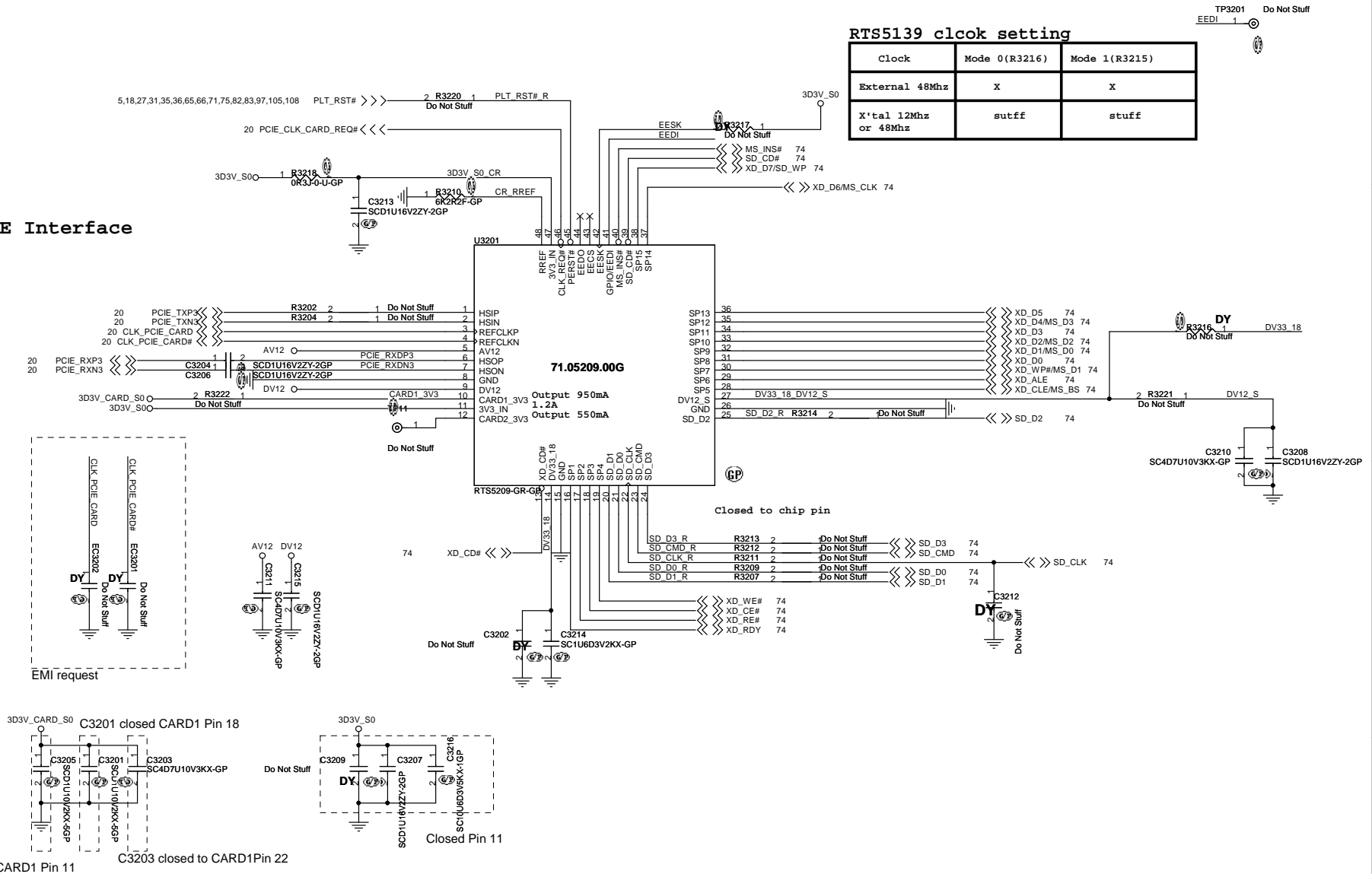
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Audio AMP		
Size	Document Number	Rev
A4	BA40-HR	SD
Date: Thursday, April 07, 2011		Sheet 30 of 109



RTS5209==>PCI-E Interface

RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	stuff	stuff



D12G

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Title	Author	Date	Page
Title	Author	Date	Page

RTS5209(CARD READER)

Size

Size	Document Number
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A3

Date: Thursday, April 07, 2011

BAD50-HR

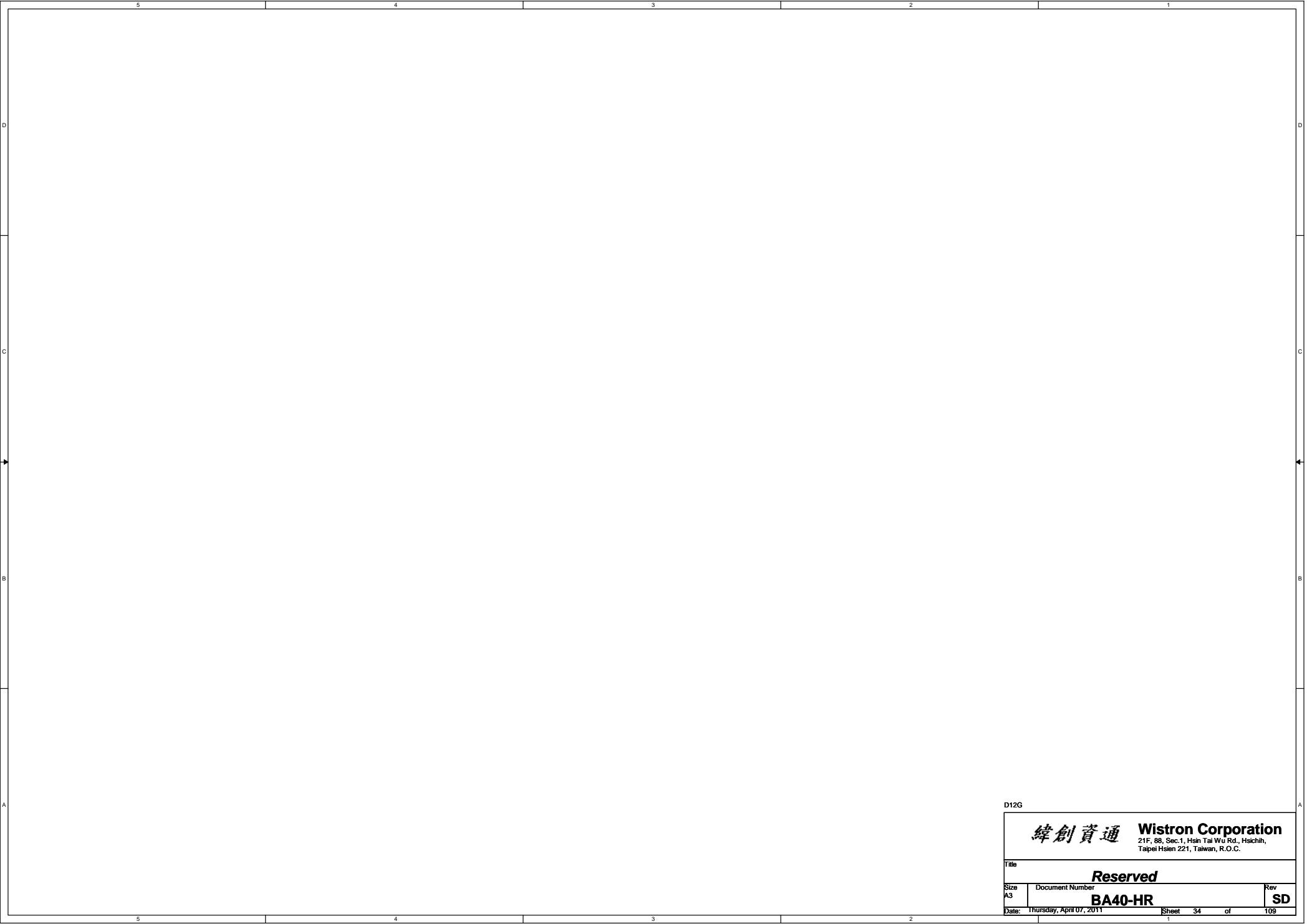
Date:

Sheet	32	of	109
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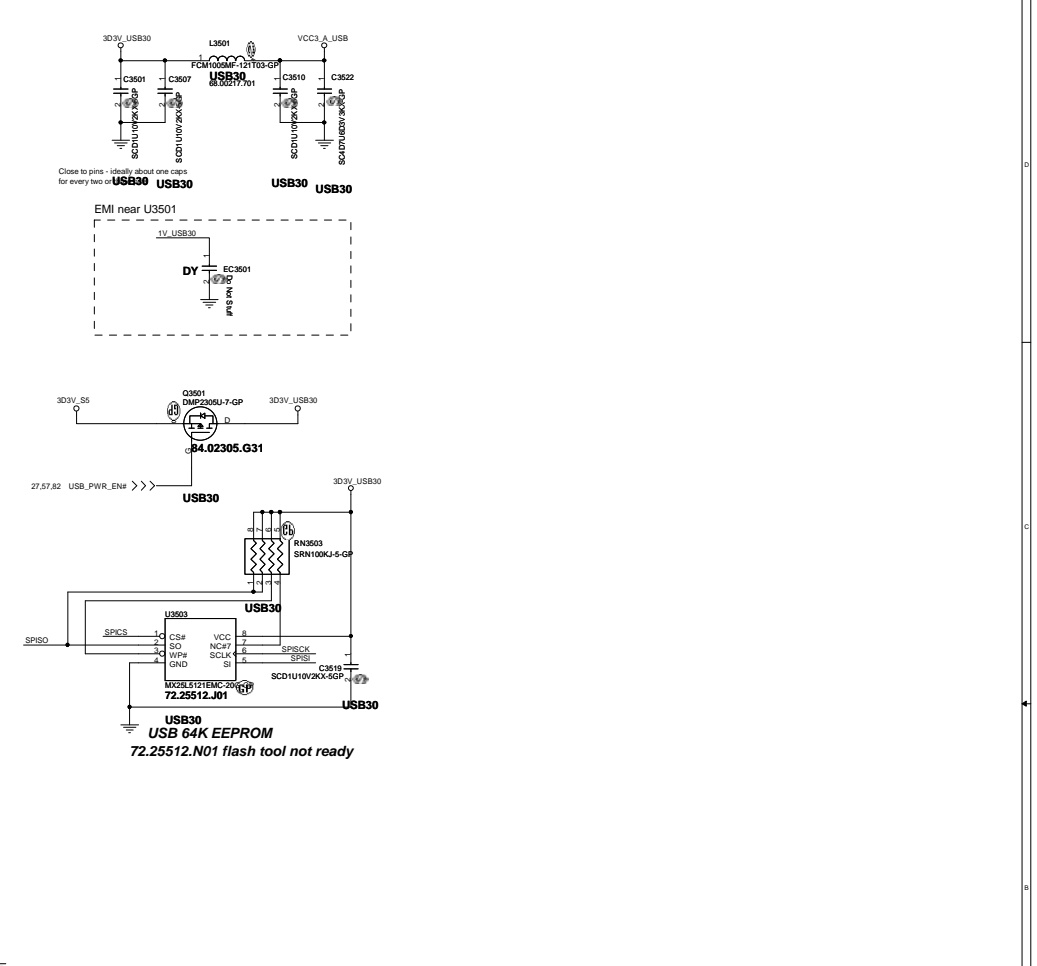
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D12G

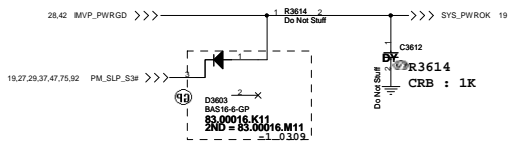
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Reserved	
Size	Document Number
A4	BA40-HR
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Sheet	33 of 109
Rev	
SD	



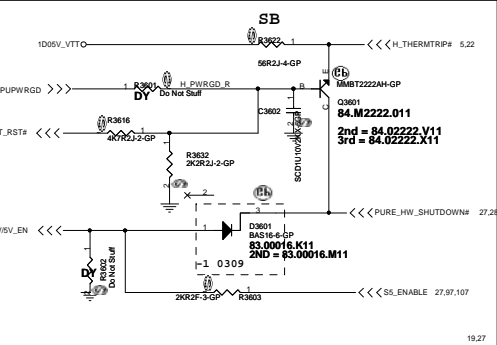
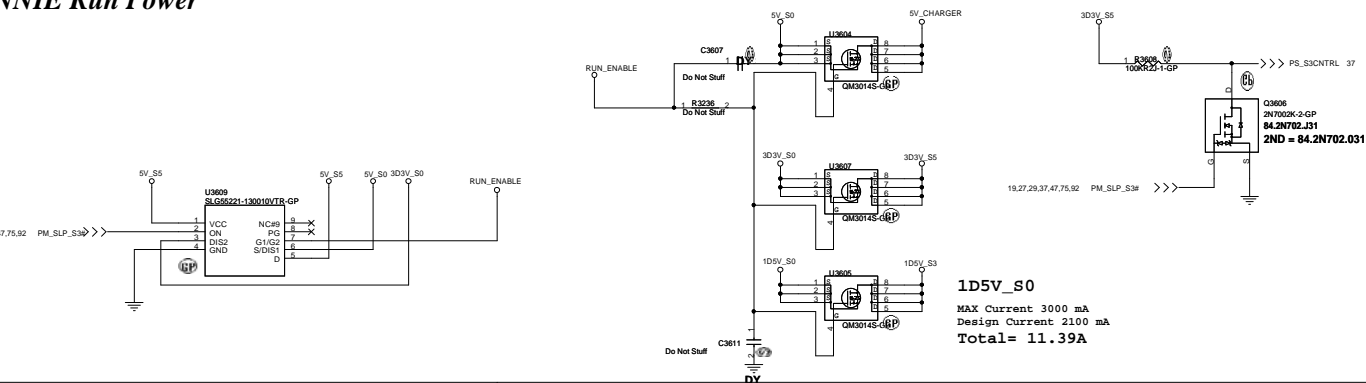
D12G		
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Title		
Reserved		
Size	Document Number	Rev
A3	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 34 of 109



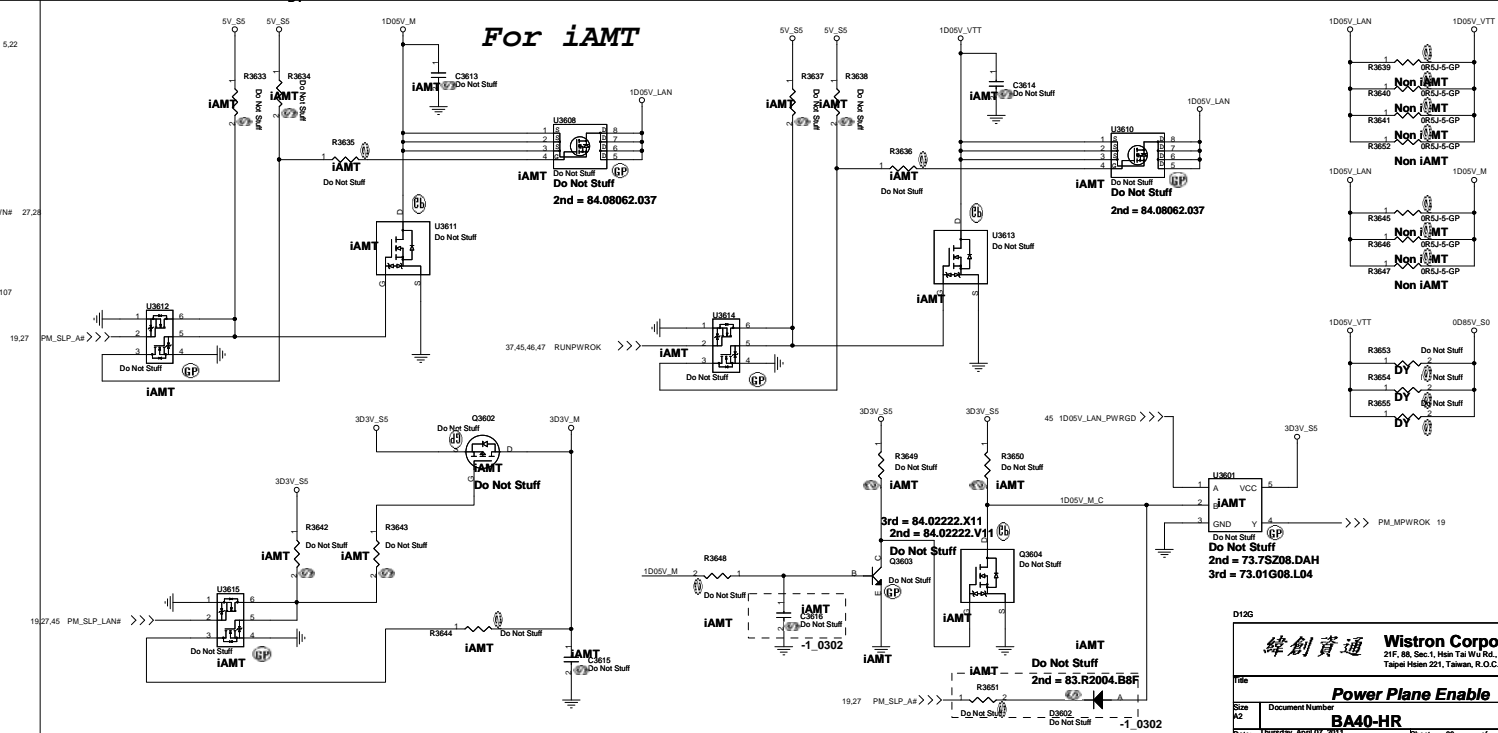
Power Sequence



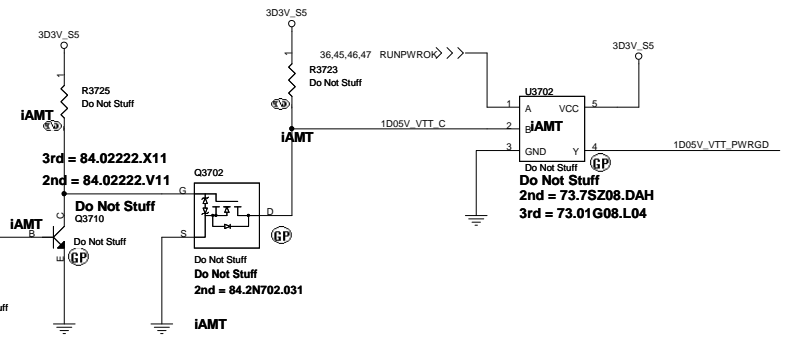
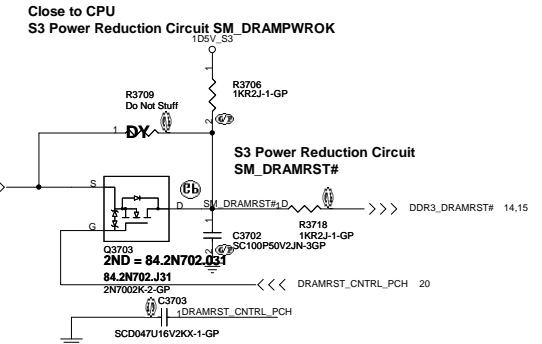
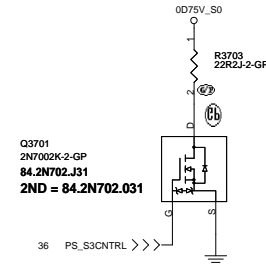
ANNIE Run Power



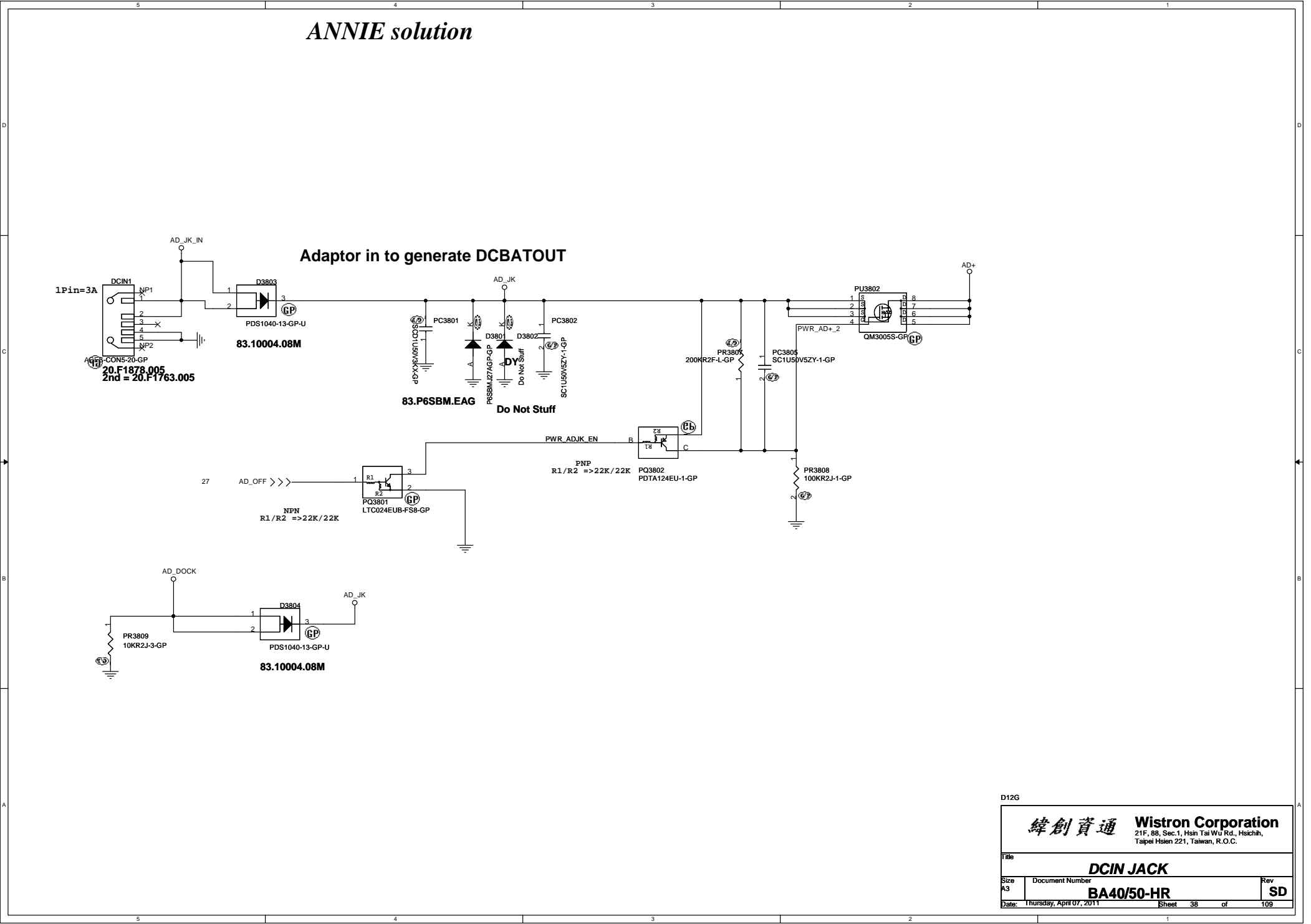
For iAMT



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



D12G

[illegible]

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN JACK

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DCIN JACK

BA40/50-HR

SD

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ANNIE solution

Adaptor in to generate DCBATOUT

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Date: Thursday, April 07, 2011 Sheet 38 of 109

[illegible]

ANNIE solution

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DCIN JACK

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Date: Thursday, April 07, 2011 Sheet 38 of 109

ANNIE solution

Adaptor in to generate DCBATOUT

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DCIN JACK

BA40/50-HR

SD

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ANNIE solution

Adaptor in to generate DCBATOUT

DCIN JACK

DCIN1

1Pin=3A

NP1

2

3

4

5

NP2

AG155-CON5-20-GP

20.F1878.005

2nd = 20.F1763.005

AD_JK_IN

D3803

PDS1040-13-GP-U

83.10004.08M

AD_JK

PC3801

PC3802

SC1U50V5ZY-1-GP

83.P6SBM.EAG

D3801

D3802

Do Not Stuff

PWR_ADJ_EN

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3807

200KR2F-L-GP

PR3805

SC1U50V5ZY-1-GP

PWR_AD+_2

QM3005S-GP

PU3802

AD+

PR3808

100KR2J-1-GP

AD_DOCK

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

R1/R2 => 22K/22K

PQ3802

PDTA124EU-1-GP

PR3808

100KR2J-1-GP

PR3809

10KR2J-3-GP

D3804

PDS1040-13-GP-U

83.10004.08M

AD_JK

27

AD_OFF >>>

NPN

R1/R2 => 22K/22K

PO3801

LTC024EUB-FS8-GP

PNP

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN JACK

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Taipei Hsien 221, Taiwan, R.O.C.

DCIN JACK

BA40/50-HR

SD

Date: Thursday, April 07, 2011 Sheet 38 of 109

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN JACK

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

DCIN JACK

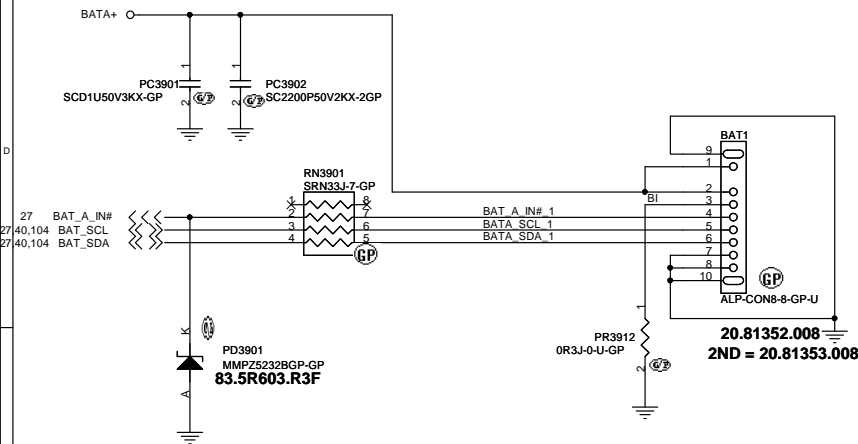
BA40/50-HR

SD

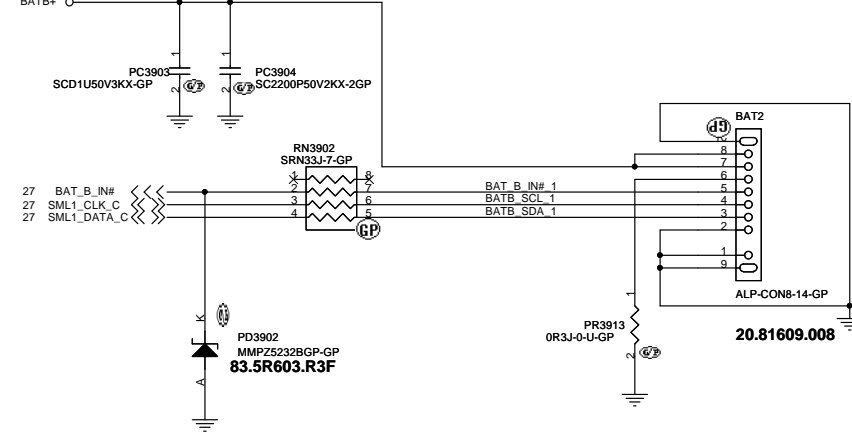
Date: Thursday, April 07, 2011 Sheet 38 of 109

[illegible][illegible][illegible]

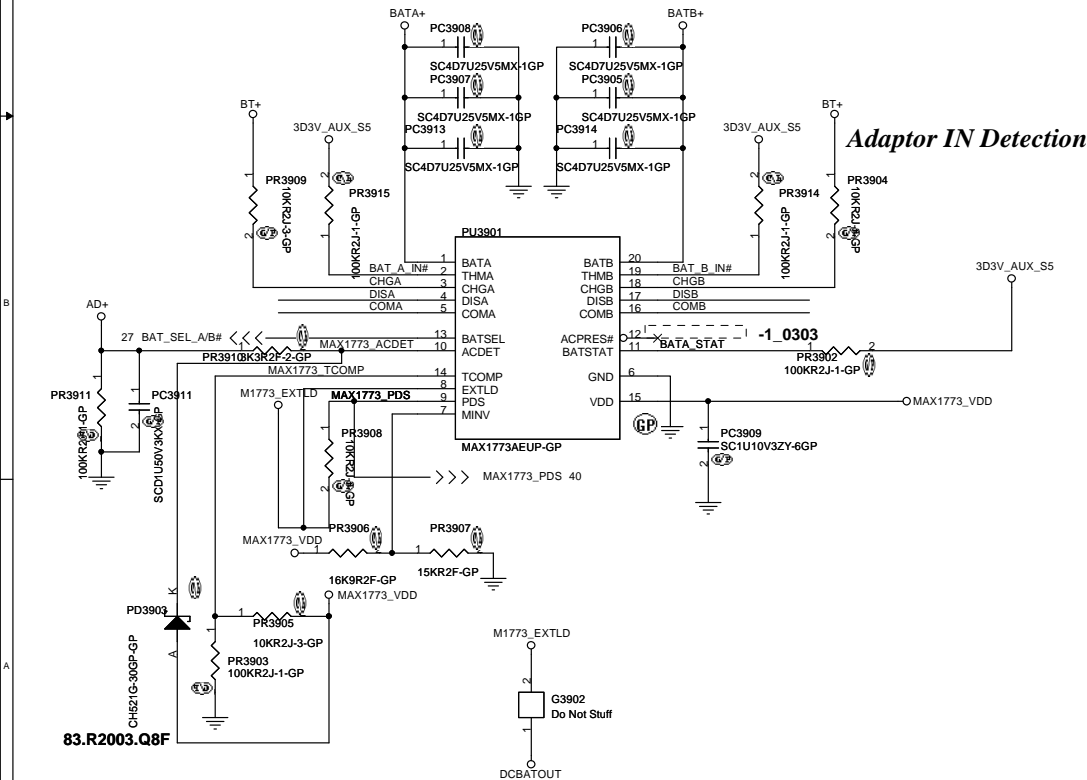
MAIN BATTERY CONNECTOR



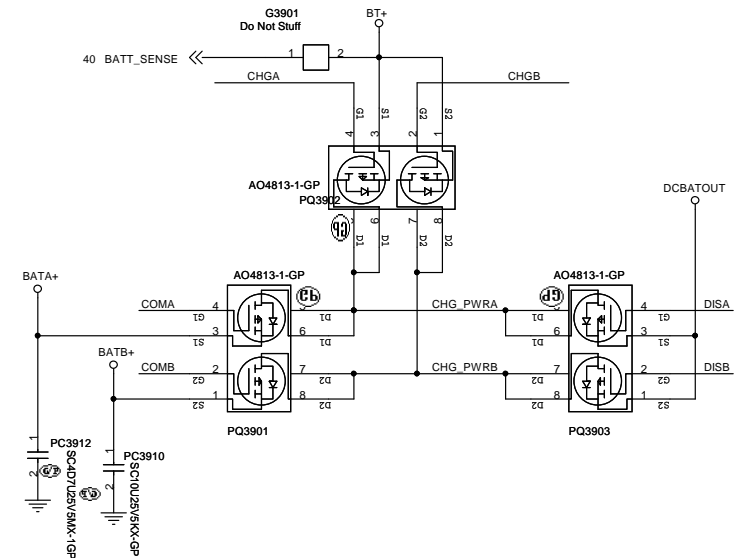
2nd BATTERY CONNECTOR



BATTERY SWITCH



Adaptor IN Detection



D12G

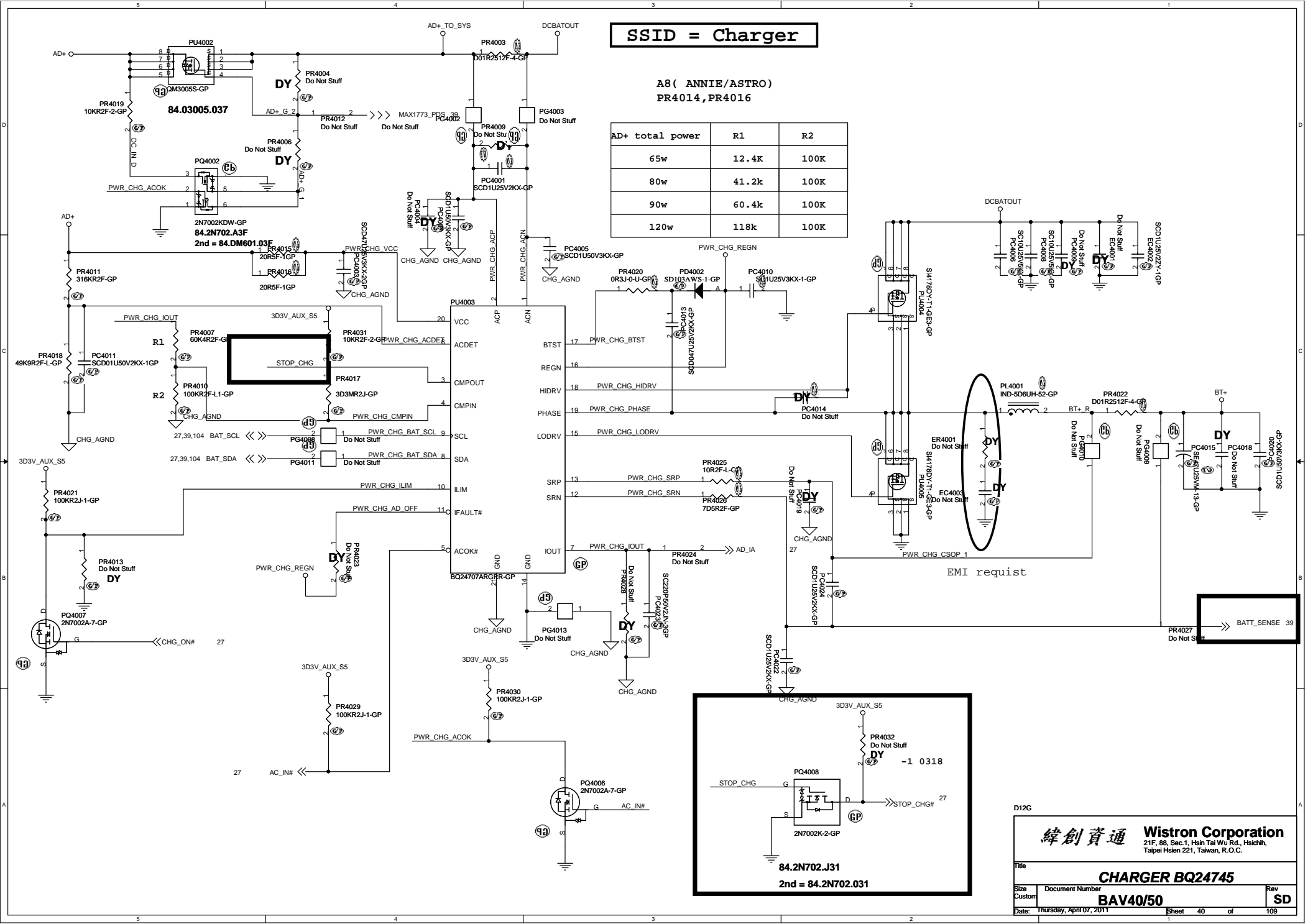
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

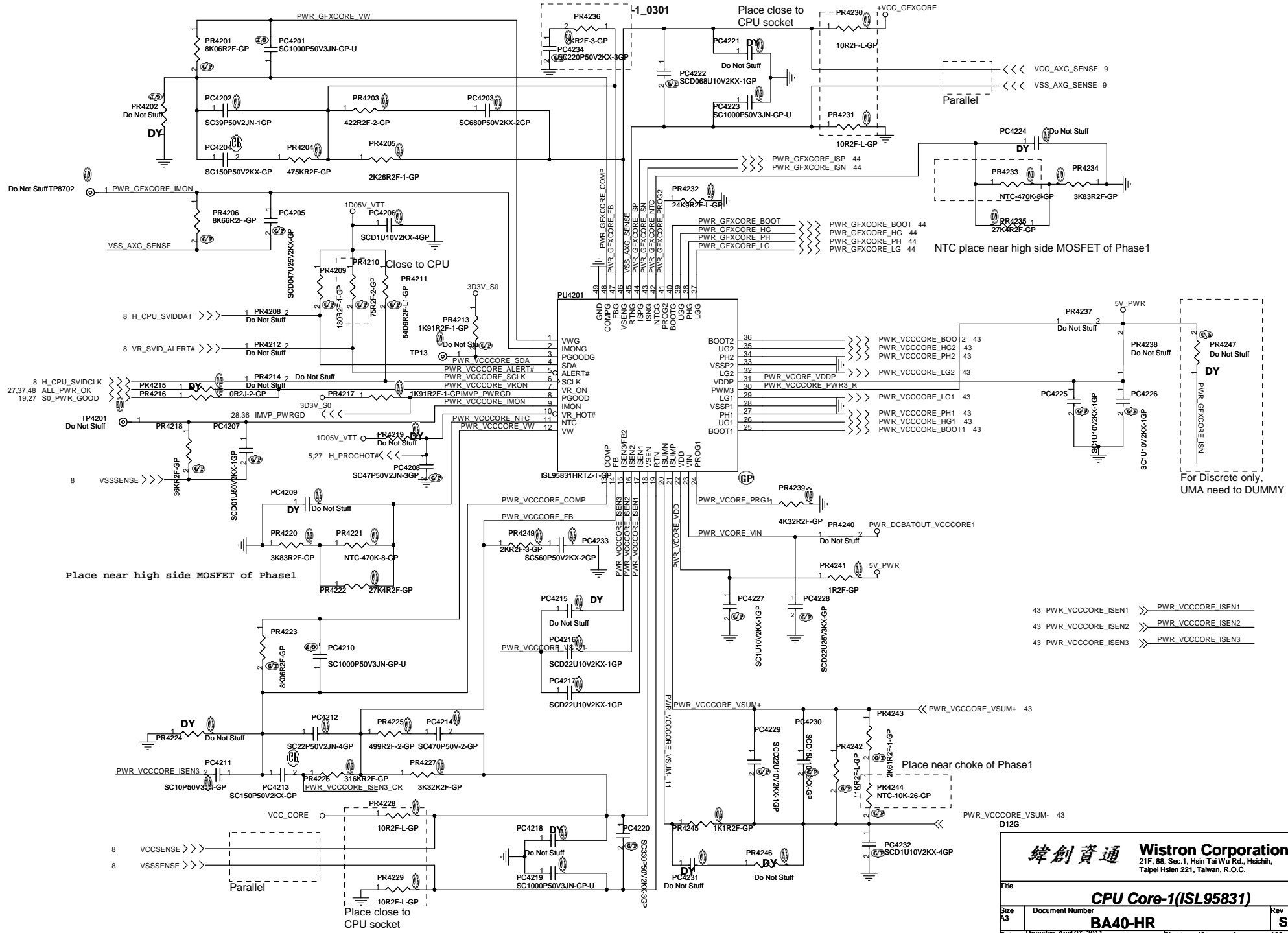
Title		
BATT CONN		
Size	Document Number	Rev
A3	BA40/50-HR	SD
Date: Thursday, April 07, 2011 Sheet 39 of 109		

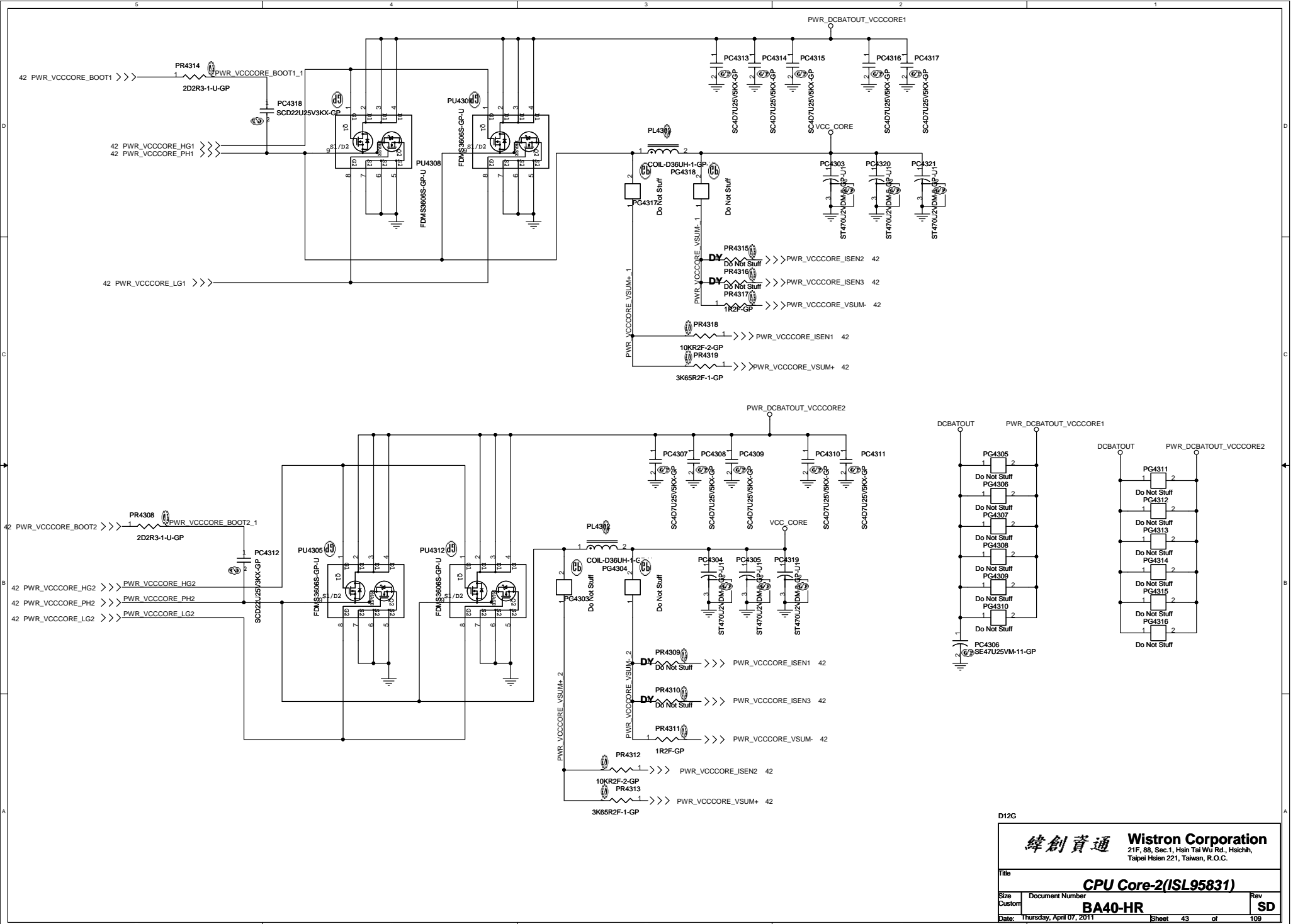
SSID = Charger

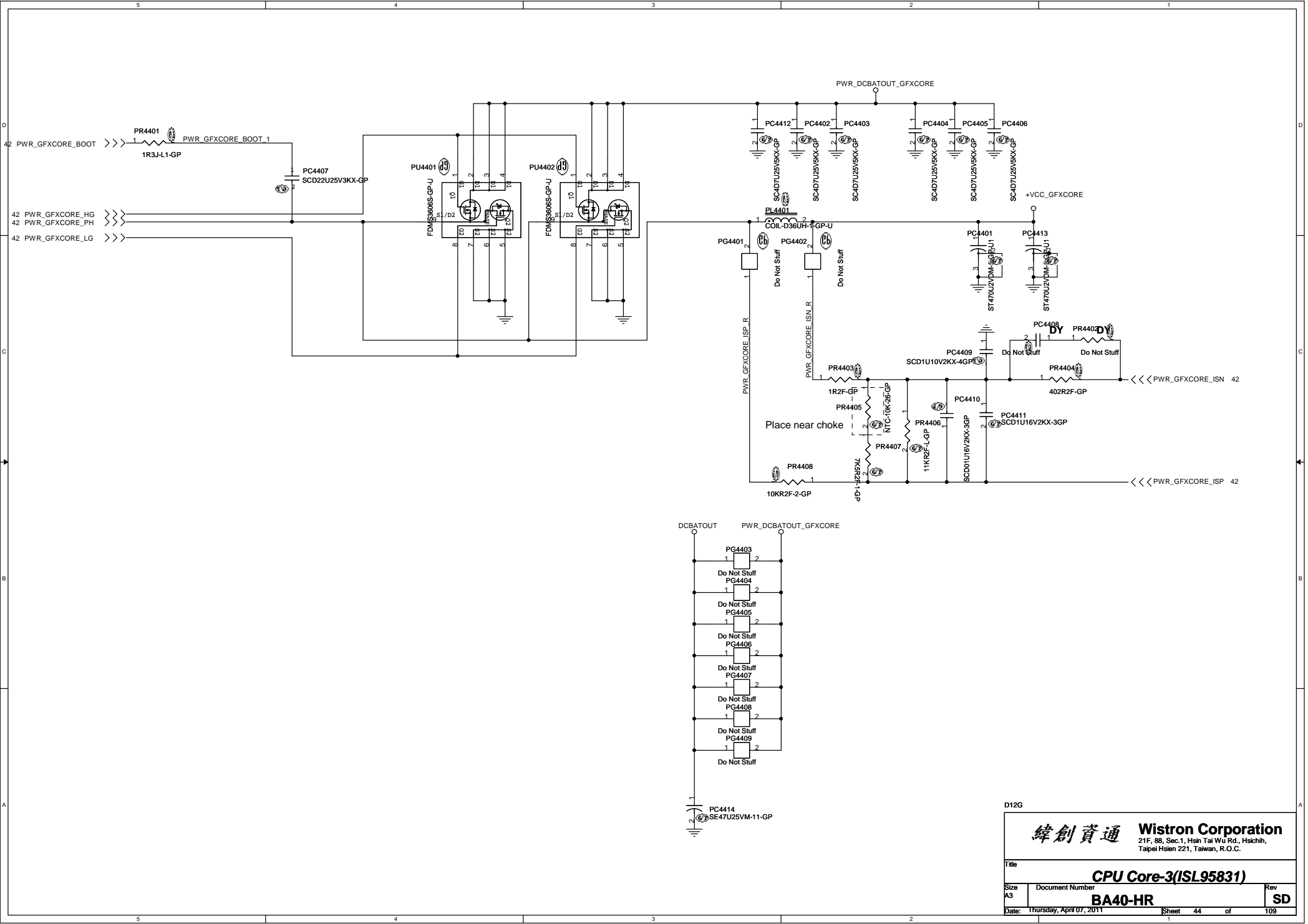
A8(ANNIE/ASTRO)
PR4014, PR4016

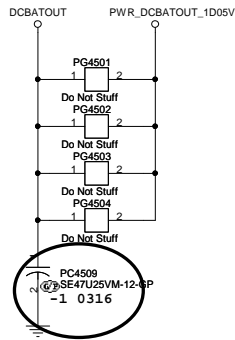
AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



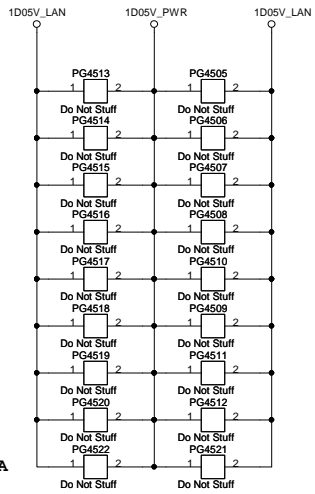
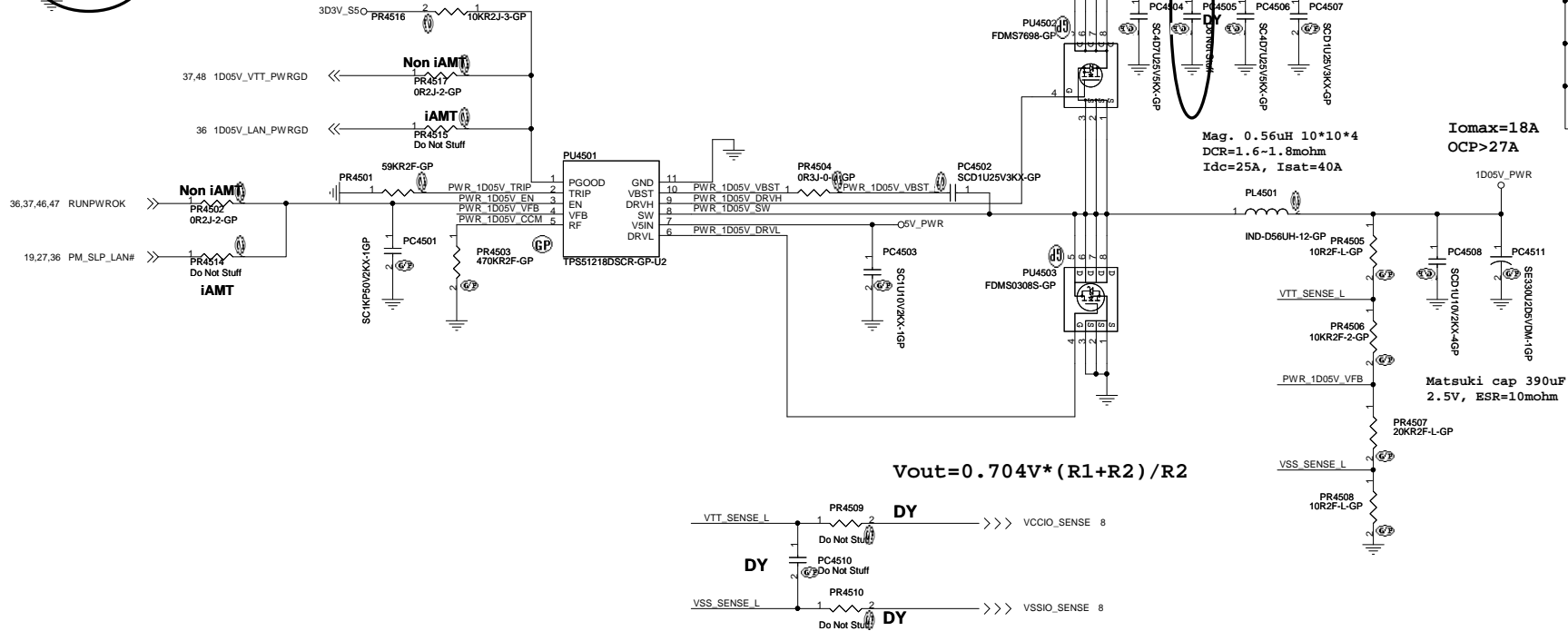








TPS51218 for 1D05V



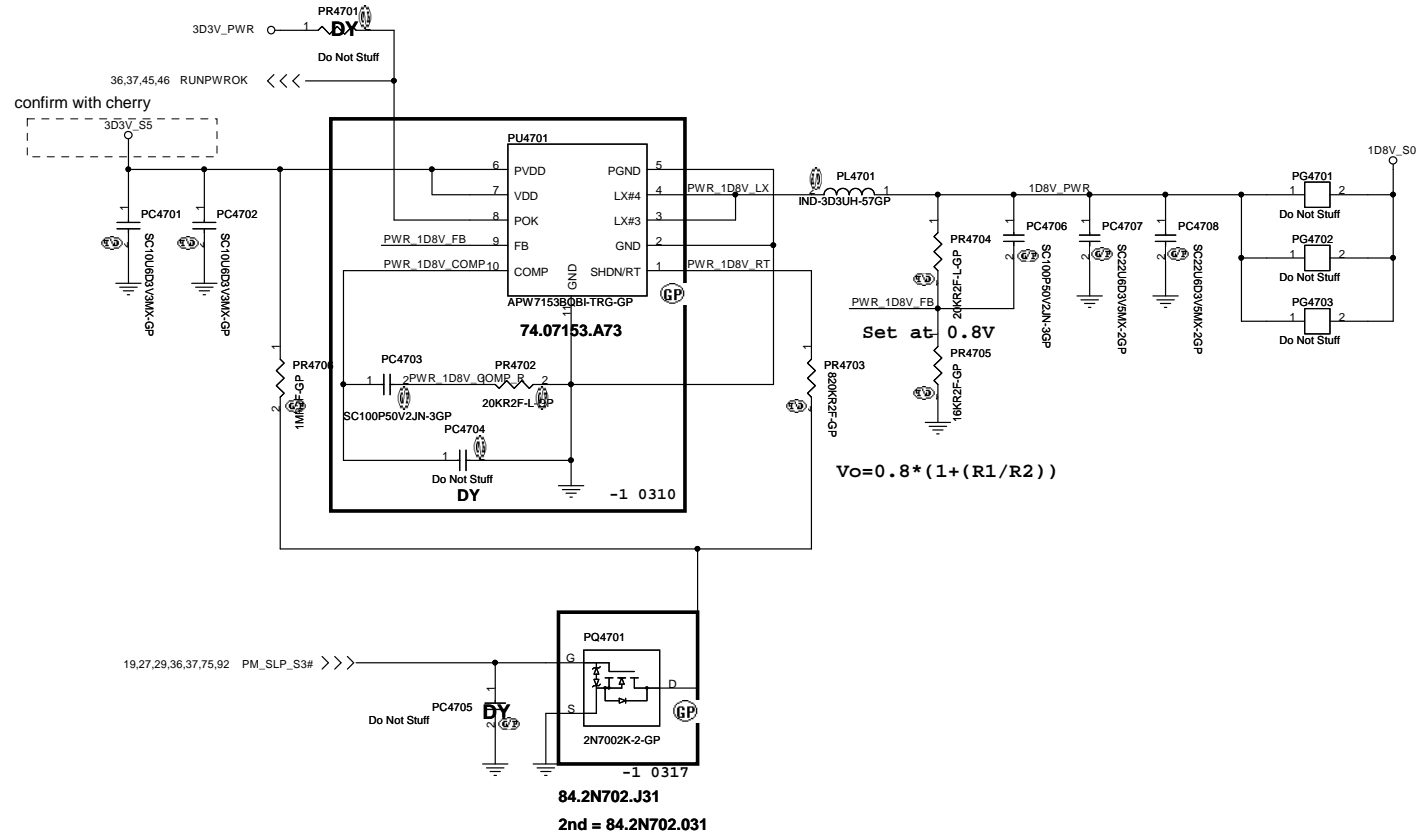
D12G

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC to DC 1D05V(TPS51218D)			
Size	Document Number	Rev	
Custom	BA40/50-HR	SD	
Date:	Thursday, April 07, 2011	Sheet	45 of 109

[illegible]

RT8015B for 1D8V_S0

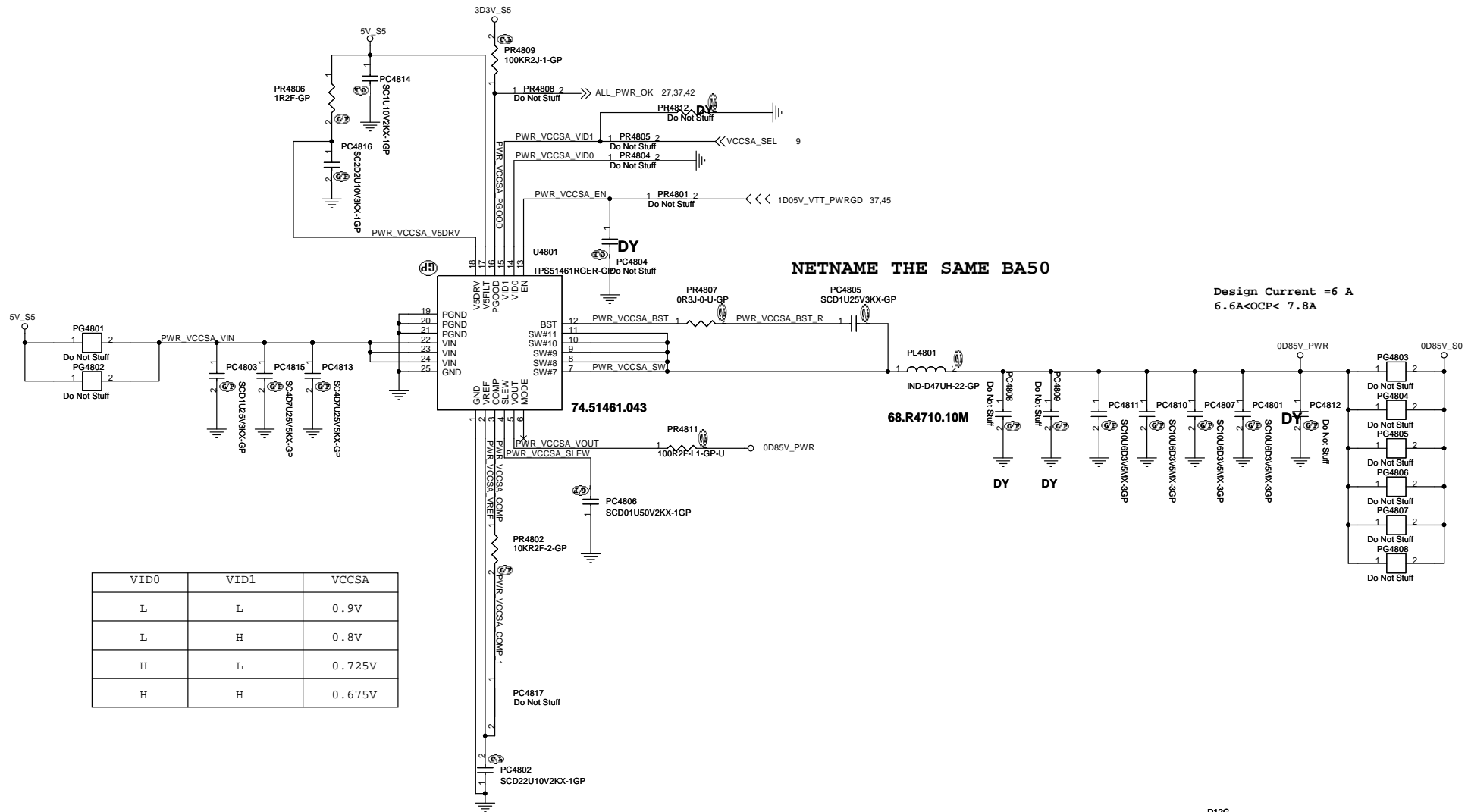


D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
LDO 1D8V(RT8015)				
Size A3	Document Number			Rev
	BA40/50-HR			SD
Date:	Thursday, April 07, 2011		Sheet 47 of	109

TPS51461 for VCCSA



D12G

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Taipei Hsien 221, Taiwan, R.O.C.

	Title
--	-------

LDO_VCCSA(APL5916)

Size
A3

Document Num

BA40/50-HR

Rev
SD

Date: Thursday, April 07, 2011

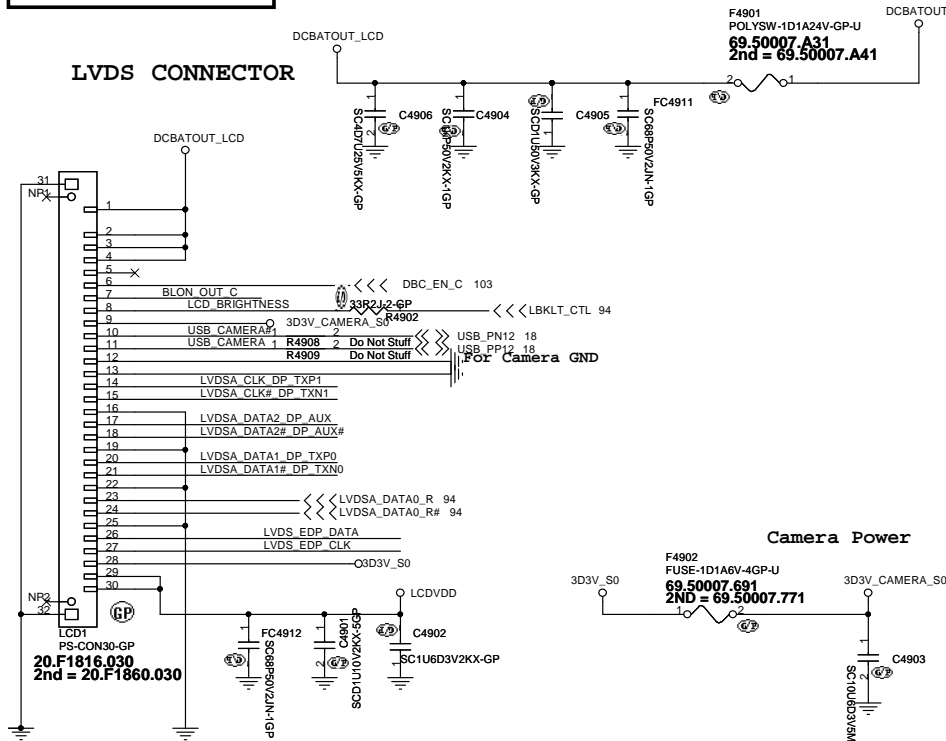
Sheet 48

of	109
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SSID = VIDEO

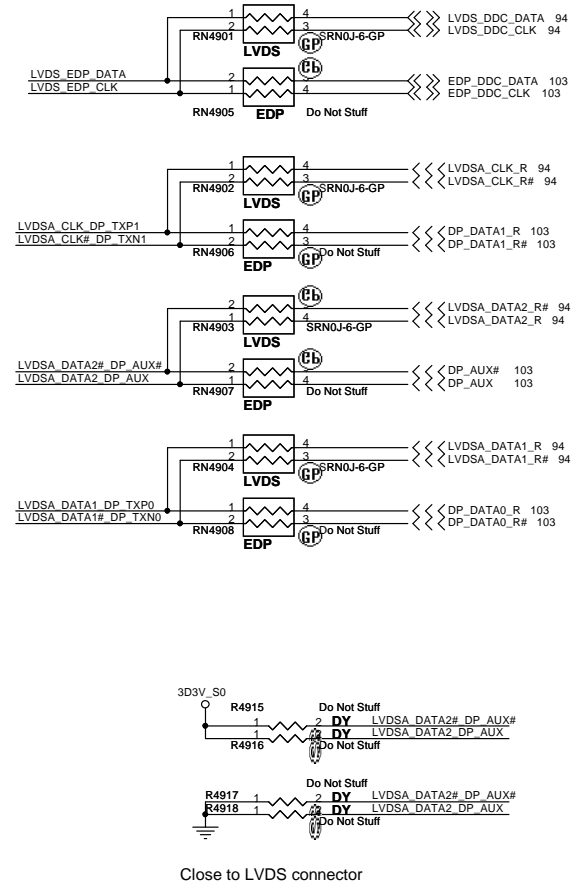
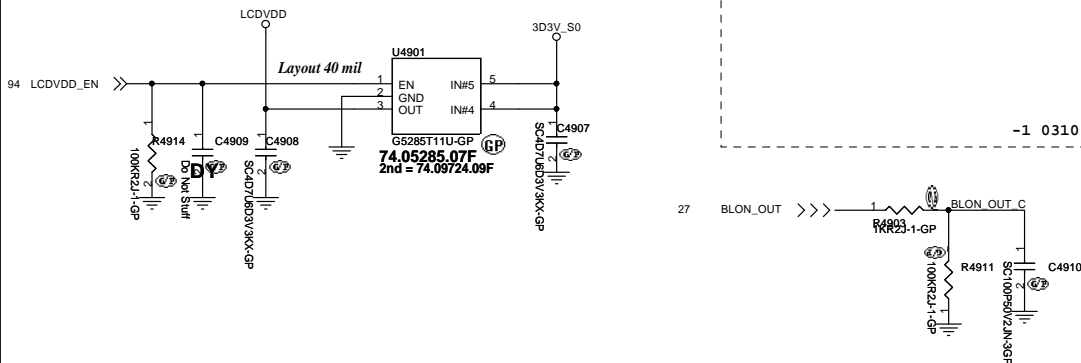
INVERTER POWER

LVDS CONNECTOR



SSID = VIDEO

LCD POWER for ANNIE



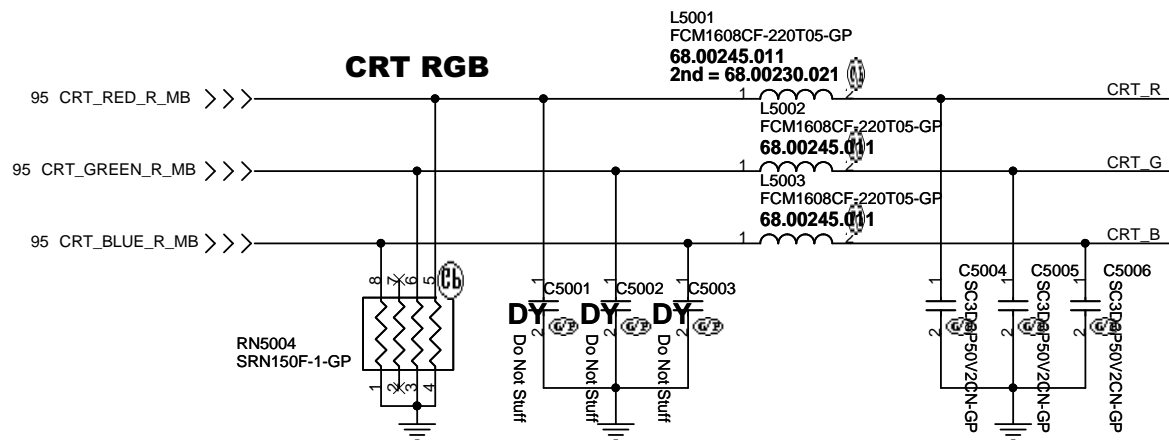
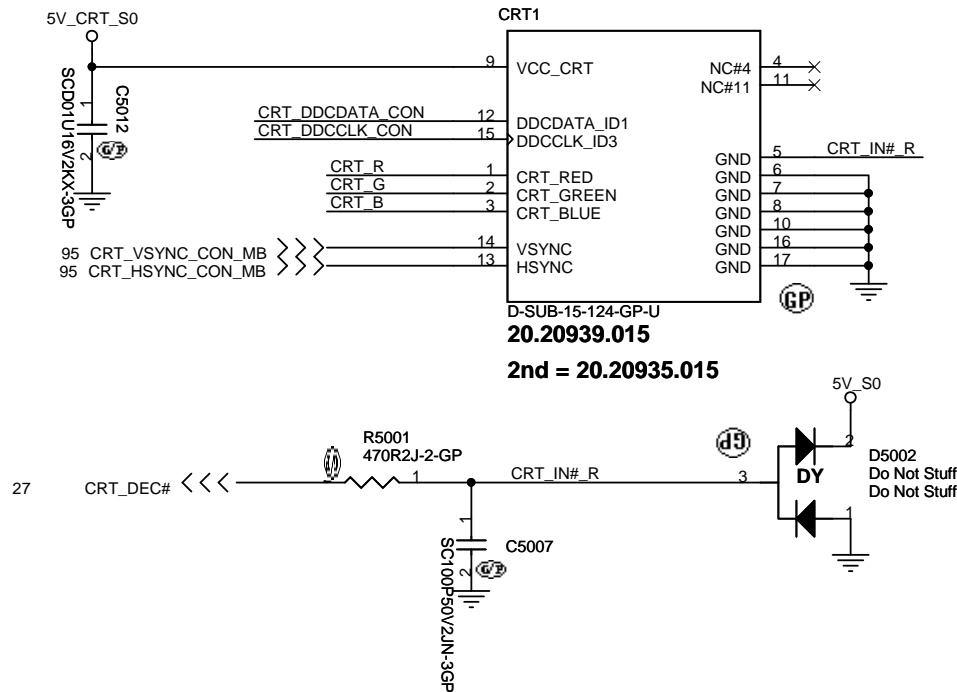
Close to LVDS connector

LVDSA_CLK_DP_TXP1	2	1 FC4901	Do Not Stuff
LVDSA_CLK# DP_TXN1	DY	1 FC4902	Do Not Stuff
LVDSA_DATA2# DP_AUX	DY	1 FC4903	Do Not Stuff
LVDSA_DATA2# DP_AUX#	DY	1 FC4904	Do Not Stuff
LVDSA_DATA1# DP_TXP0	DY	1 FC4905	Do Not Stuff
LVDSA_DATA1# DP_TXN0	DY	1 FC4906	Do Not Stuff
LVDSA_DATA0_R	DY	1 FC4907	Do Not Stuff
LVDSA_DATA0_R#	DY	1 FC4908	Do Not Stuff
LVDS_EDP_DATA	DY	1 FC4909	Do Not Stuff
LVDS_EDP_CLK	DY	1 FC4910	Do Not Stuff

D12G

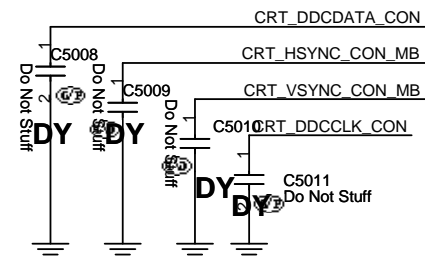
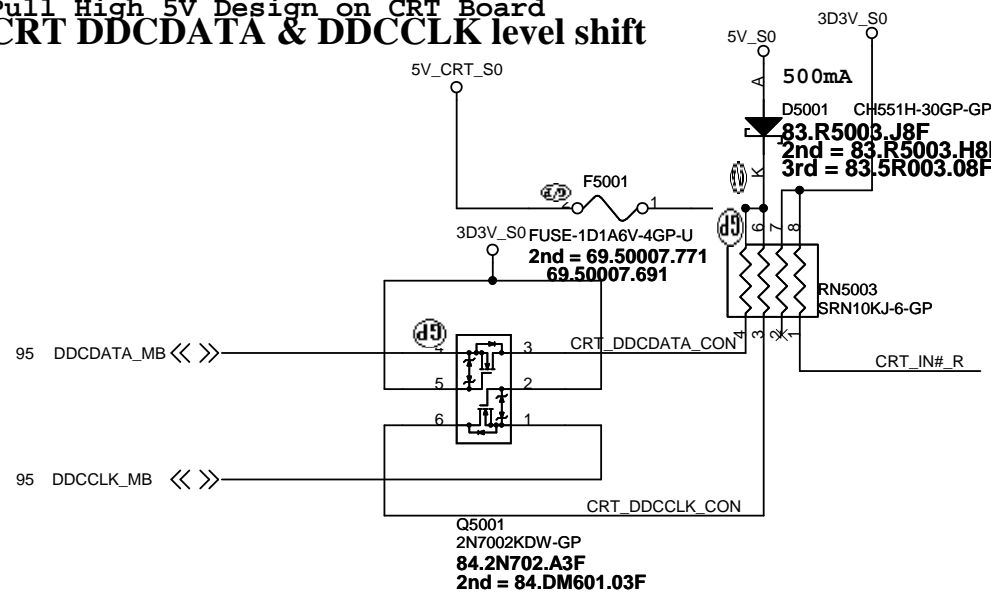
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD Connector		
Size	Document Number	Rev	SD
A3	BA40-HR		
Date:	Thursday, April 07, 2011	Sheet	49 of 109



0806 check RN5004 擺放位置

Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift



D12G

緯創資通 **Wistron Corporation**
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Title		
CRT Connector		
Size	Document Number	Rev
A4	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 50 of 109

(Blanking)

D12G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
S-VIDEO			
Size	Document Number		Rev
A4	BA40-HR		SD
Date: Thursday, April 07, 2011		Sheet 53 of	109

(Blanking)

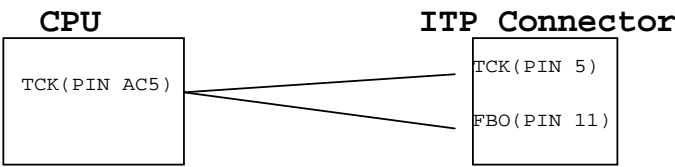
D12G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	BA40-HR		SD
Date: Thursday, April 07, 2011		Sheet 54	of 109

SSID = User.Interface

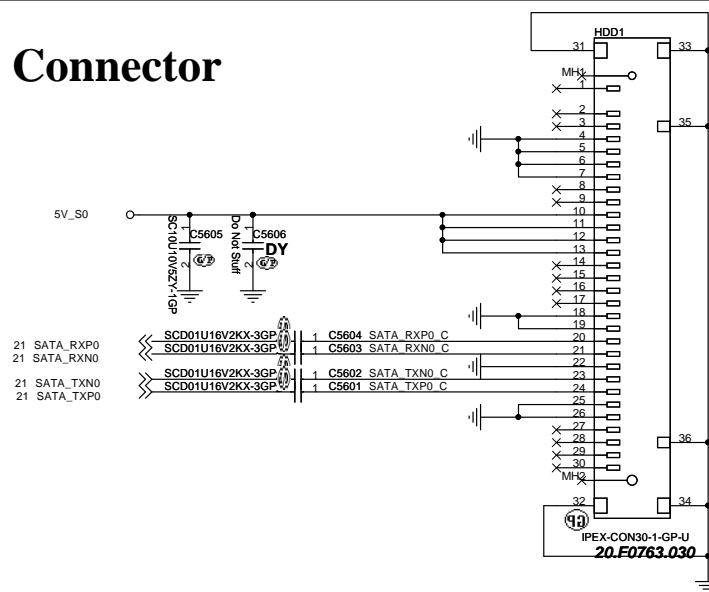
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

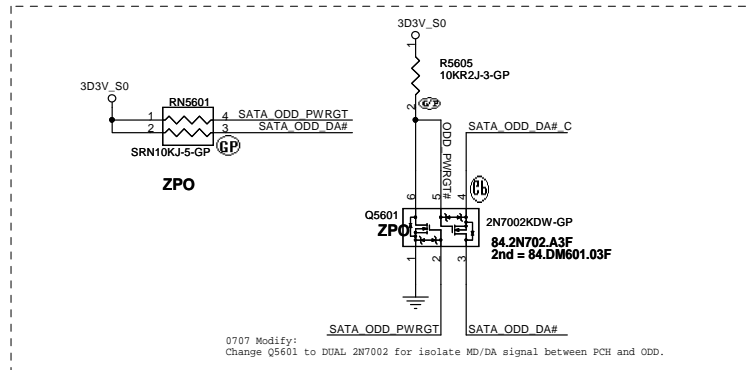
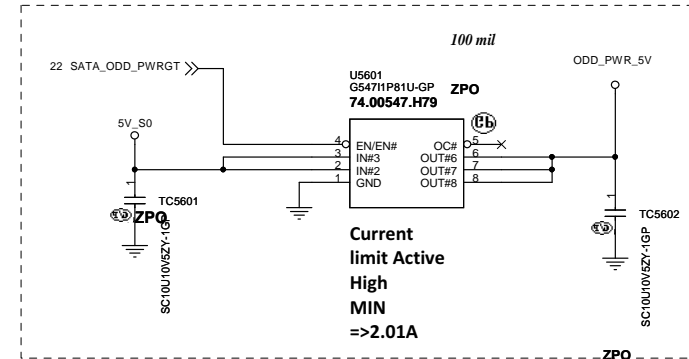
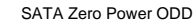
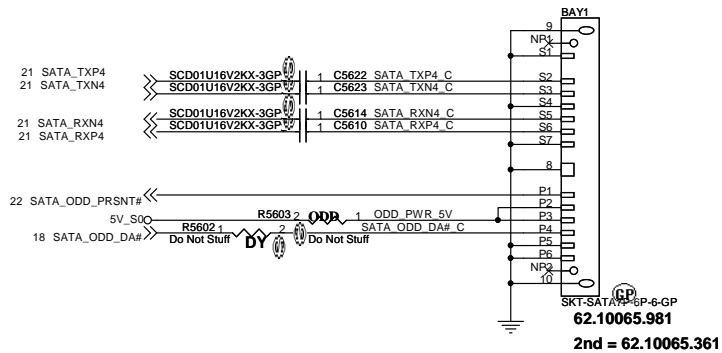


SSID = SATA

SATA HDD Connector



ODD Connector 2nd source 62.10065.541 and 62.10065.A11.



D12G

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Title

HDD/ODD

Size

Document Number

BA40-HR

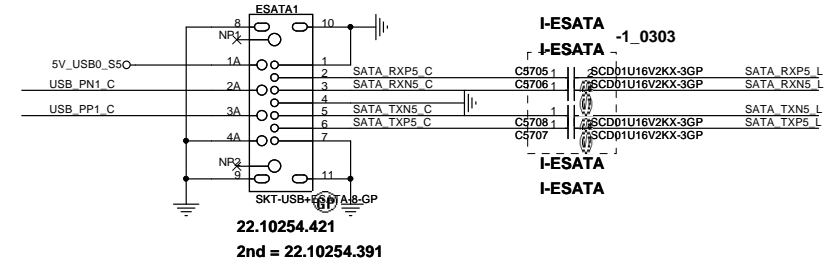
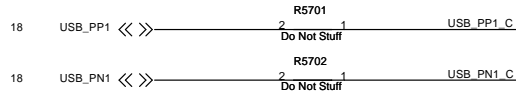
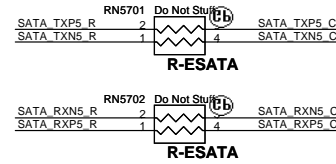
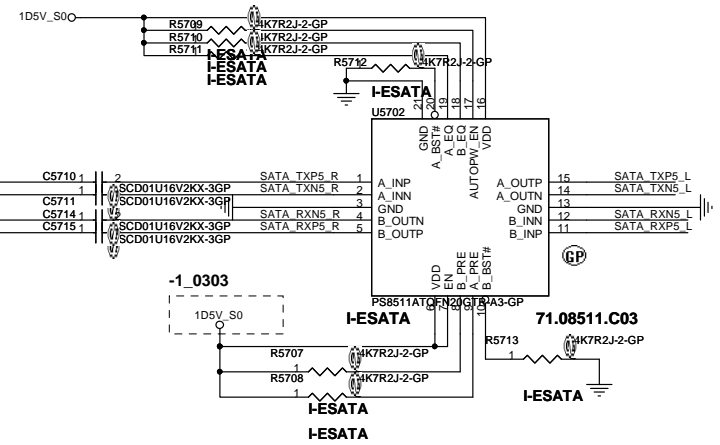
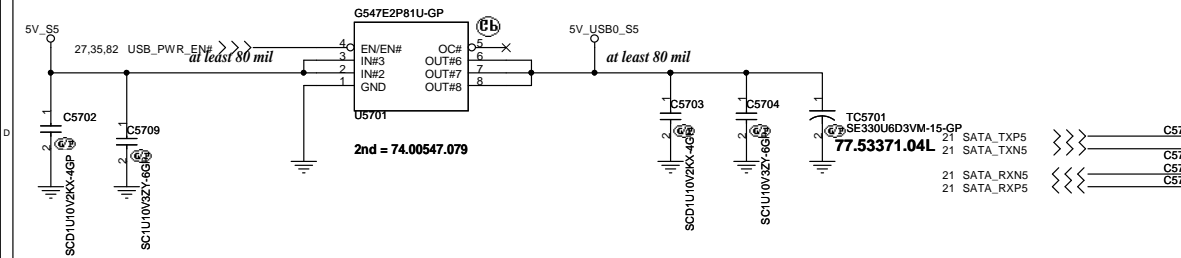
Rev

SD

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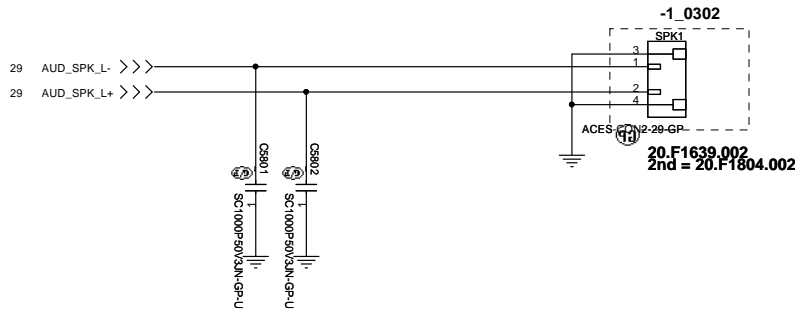
ESATA Power

```
MIN Current limit 2.5A
LOW ACTIVE TYPE!
```

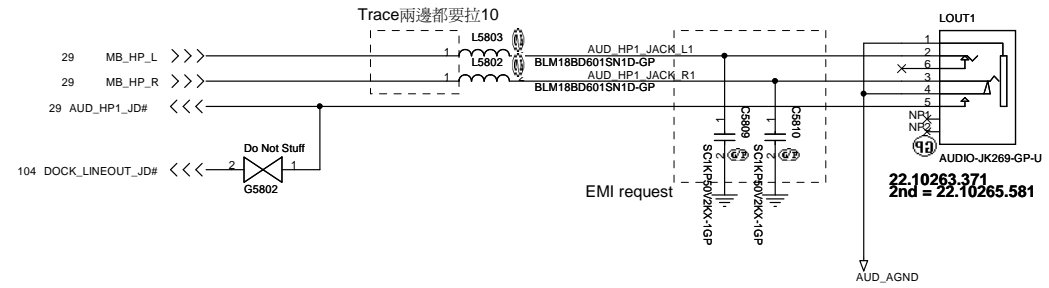


SSID = AUDIO

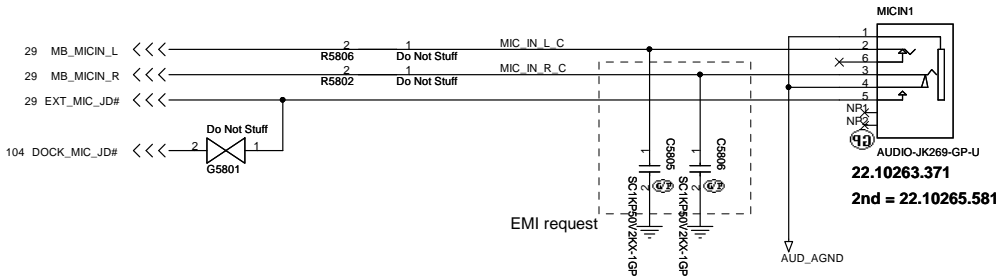
Speaker Connector



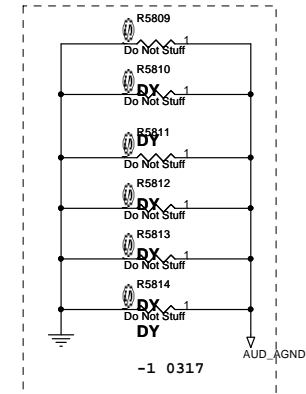
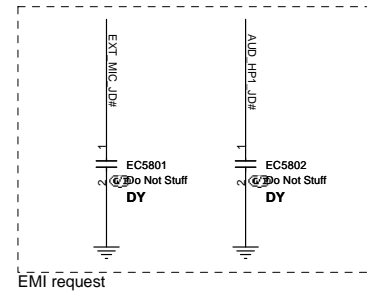
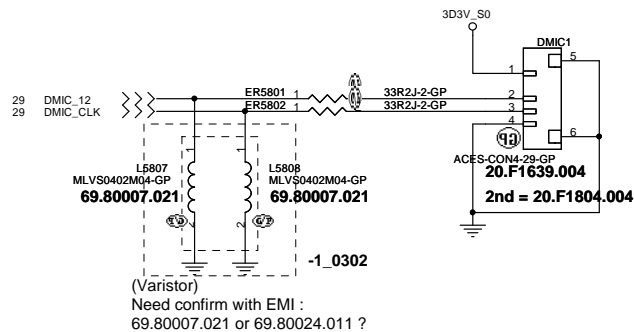
LINE1 OUT



MIC IN



Internal Microphone



D12G

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Taipei Hsien 221, Taiwan, R.O.C.

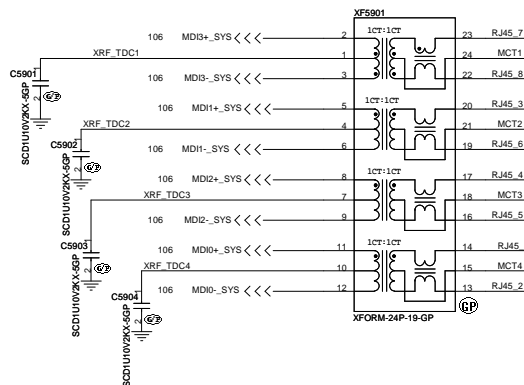
Title			Audio Jack
Size	Document Number	Rev	SA
A3	BA40-HR		
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```

106 LAN_ACT_LED#_SYS
06 10M/100M1G_LED#_SYS

```

GP ACES-CON14-1.1-GP
20.F1637.014
2nd = 20.F1808.014



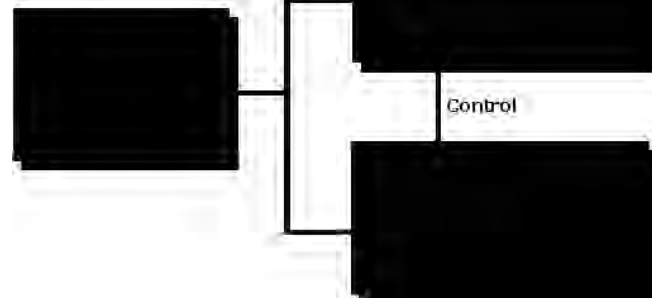
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Size	Document Number	Rev
Custom	BA40-HR	S
Date:	Thursday, April 07, 2011	Sheet 59 of 109

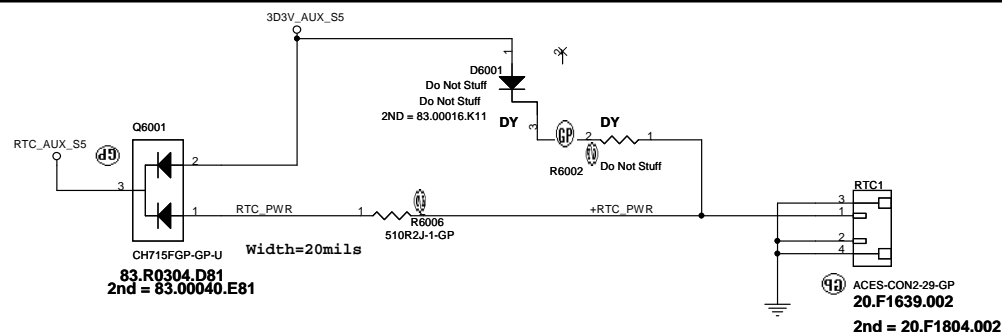
```
SSID = Flash.ROM
```



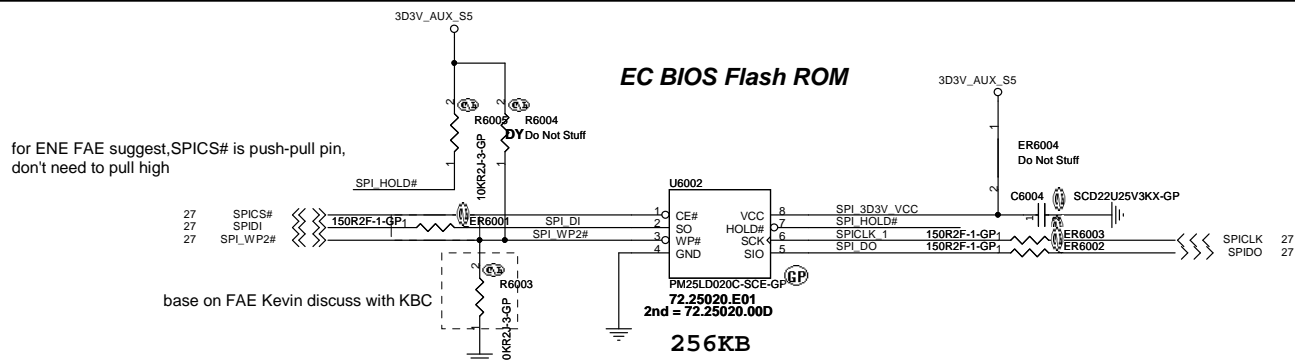
PCH and EC length less than 6.5 inch



SSID = RBATT



EC BIOS Flash ROM



D12G

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
...

Flash/RTC

Size

Document Number

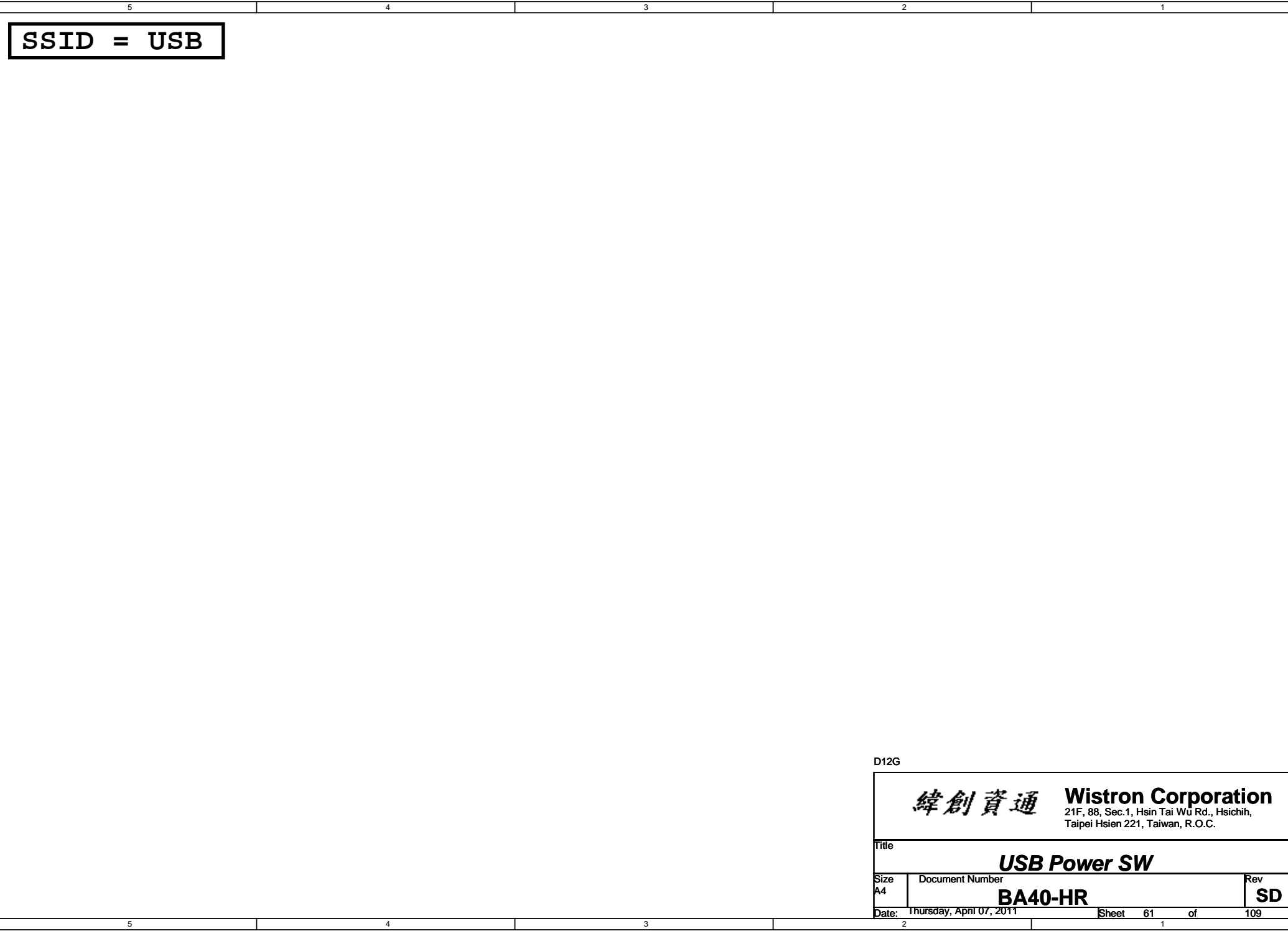
BA40-HR

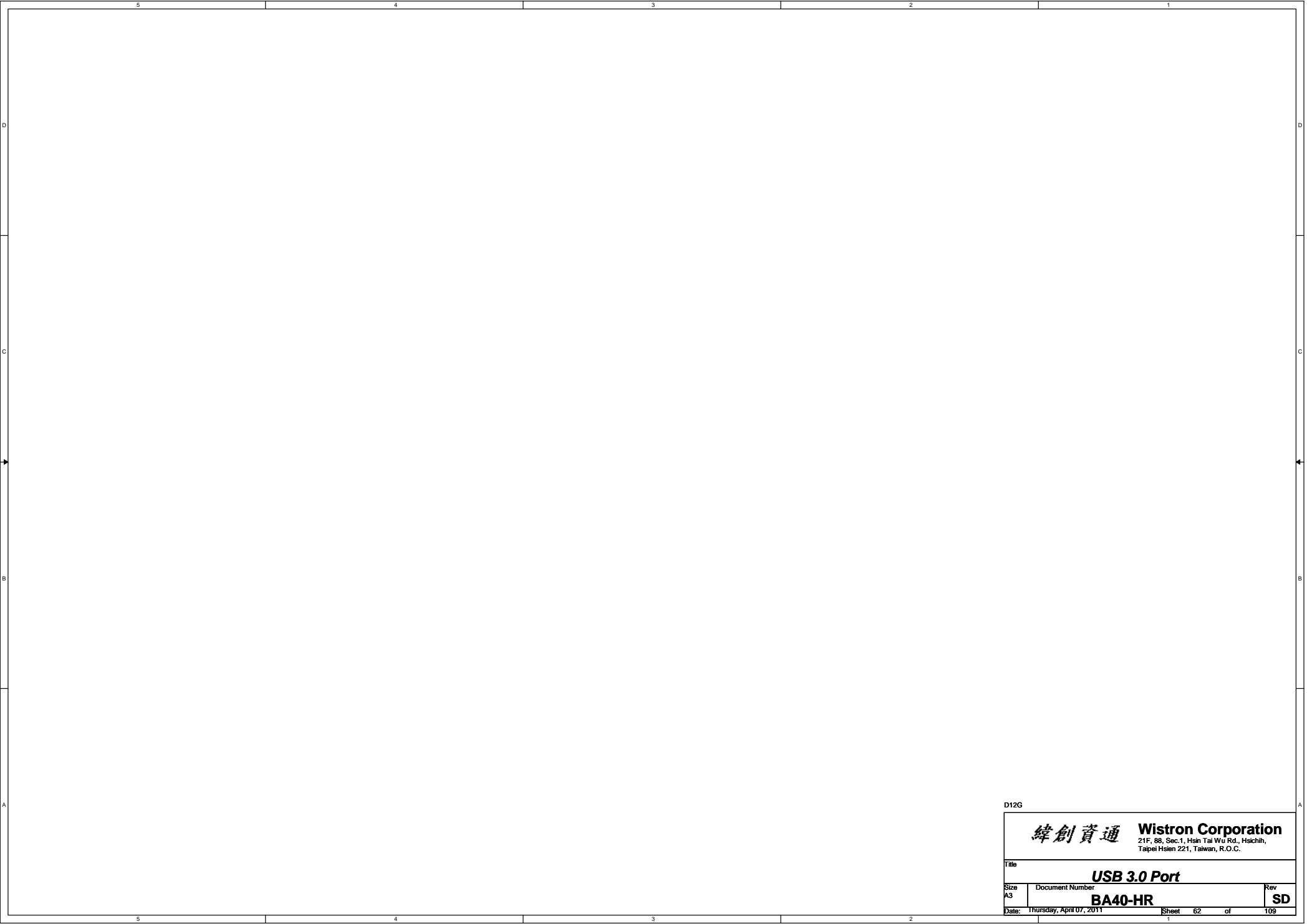
Rev

Date: Thursday, April 07, 2011

Sheet 4

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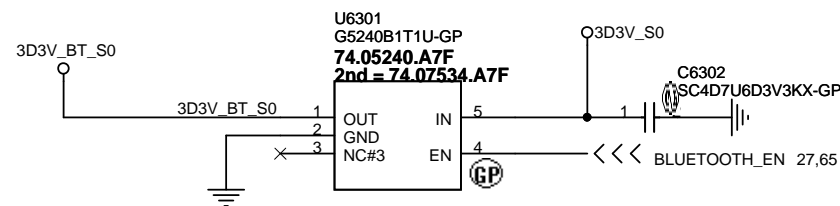




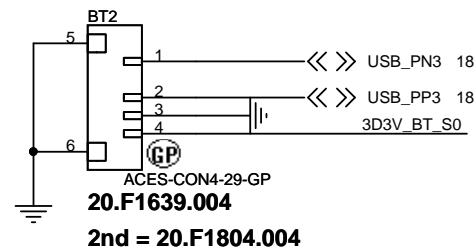
D12G		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
USB 3.0 Port		
Size	Document Number	Rev
A3	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 62 of 109

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request

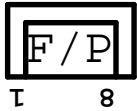


D12G

Title		Bluetooth	
Size	Document Number	Rev	
A4	BA40-HR	SD	
Date:	Thursday, April 07, 2011	Sheet	63 of 109

Finger printer

JE40 delete FP function

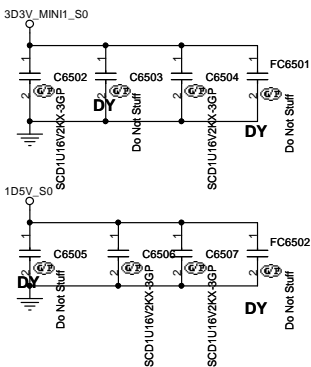
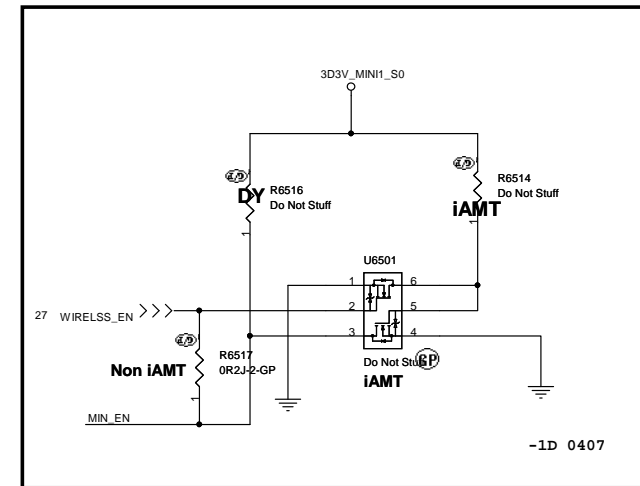
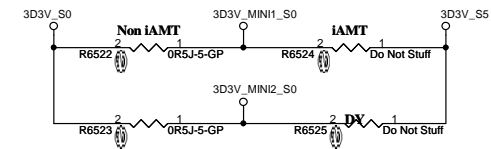
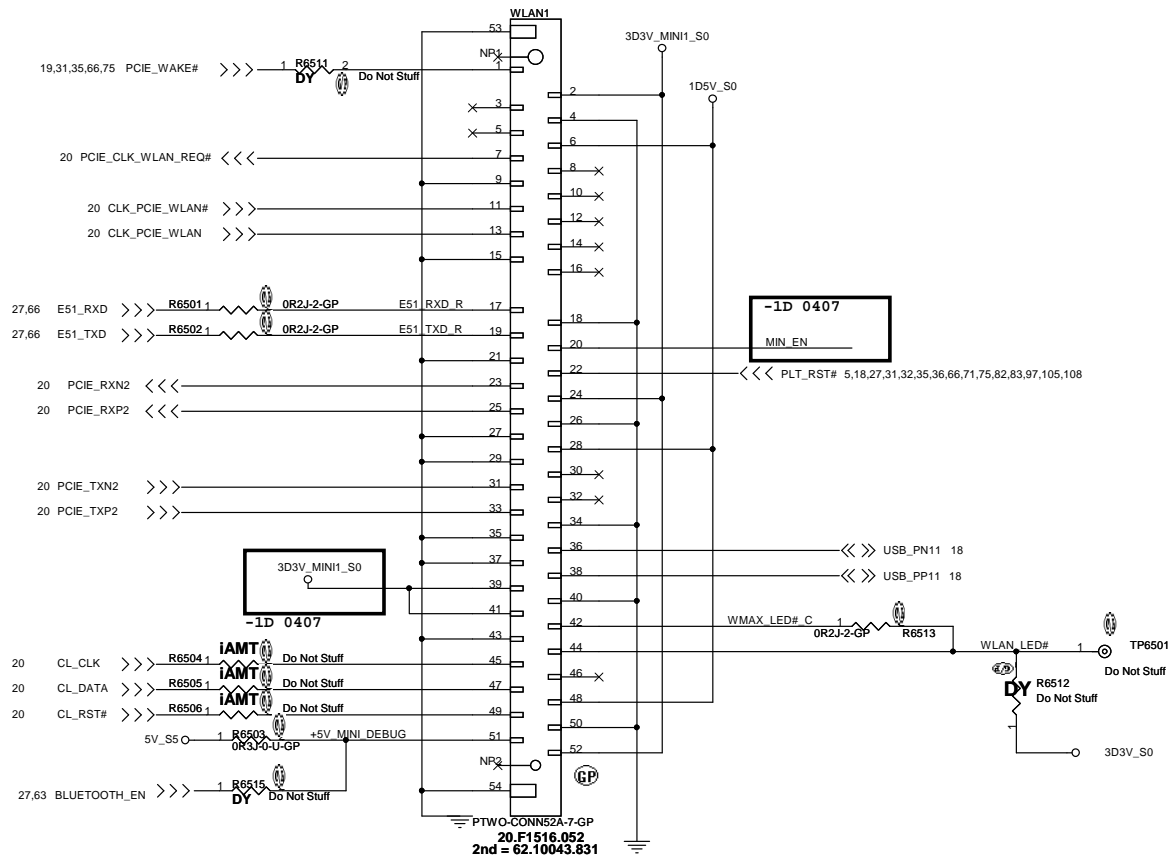


D12G

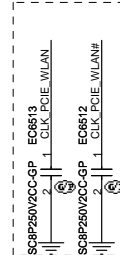
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
RESERVED	
Size	Document Number
A4	BA40-HR
Date:	Thursday, April 07, 2011
Sheet	64 of 109
Rev	SD

SSID = Wireless

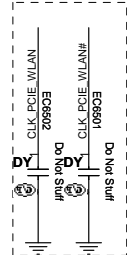
Mini Card Connector(802.11a/b/g/n)



RF suggestion



EMI request



D12G

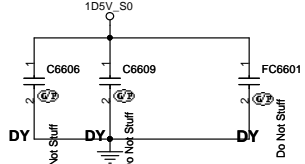
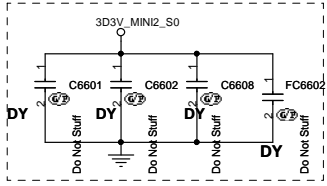
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

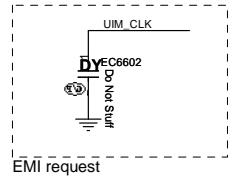
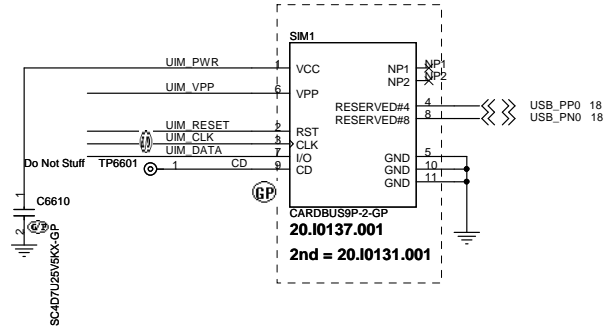
Title			MINICARD(WLAN)/TP CONN
Size	Document Number	Rev	SD
A3	BA40-HR		
Date:	Thursday, April 07, 2011	Sheet	65 of 109

SSID = Wireless

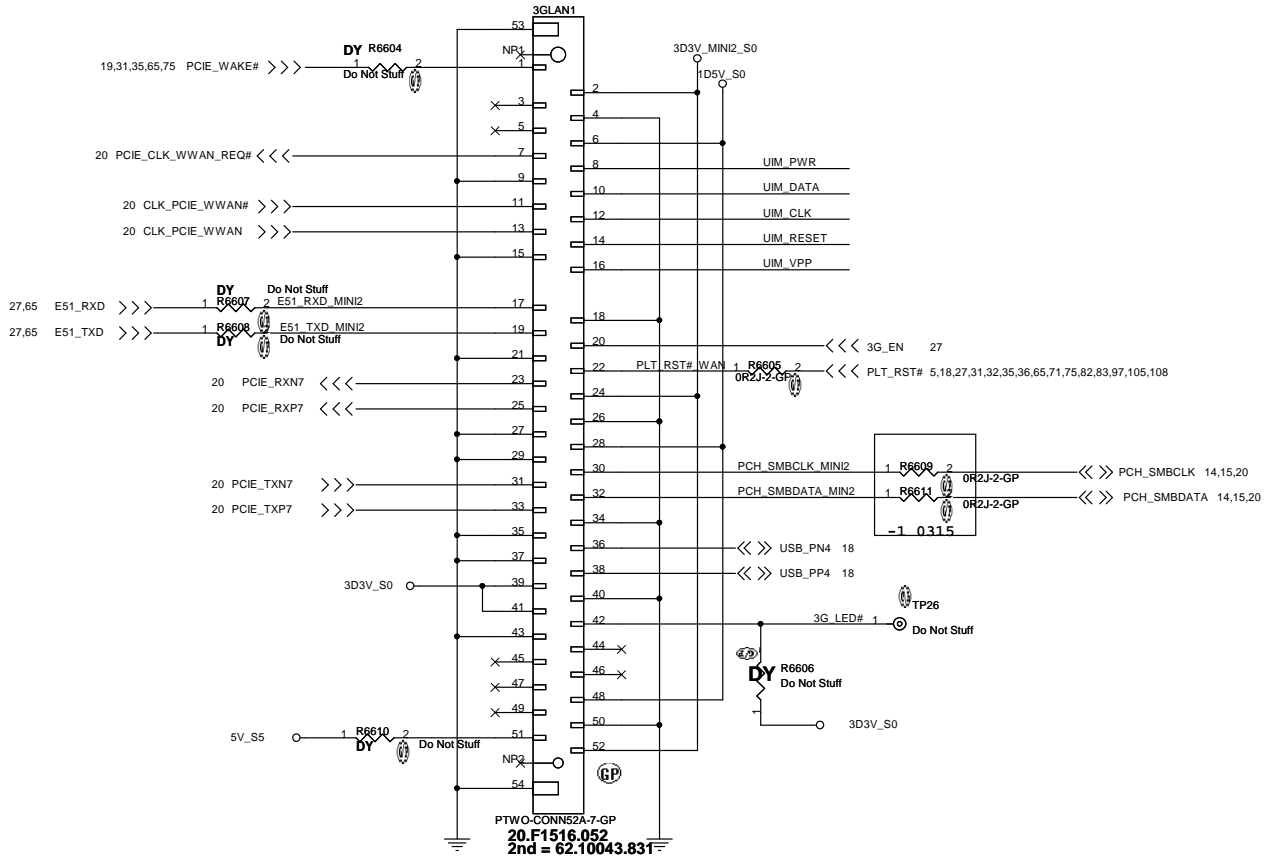
20100712 V1.5
Place near MINI Card CONN



-1_0304



Mini Card Connector(WWAN)



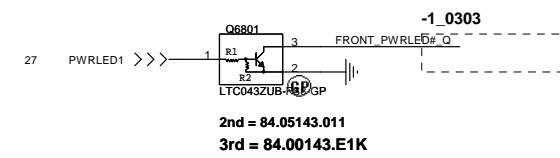
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D12G

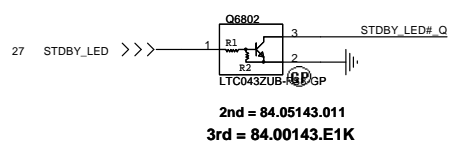
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BA40-HR	SD
Date: Thursday, April 07, 2011		Sheet 67 of 109

SSID = User.Interface

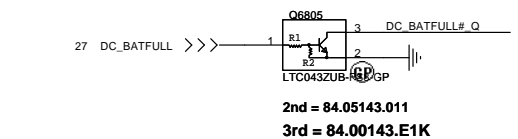
Power button LED



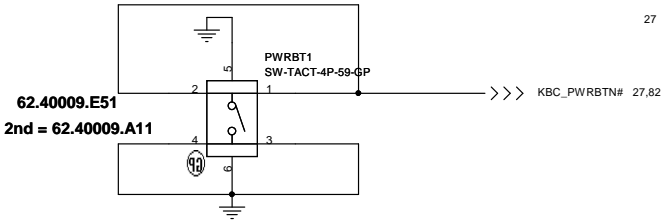
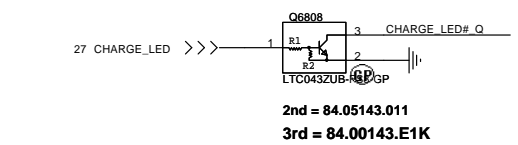
Power STDBY_LED



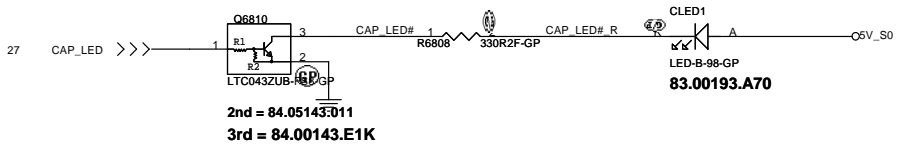
Battery LED2(DC_BATFULL)



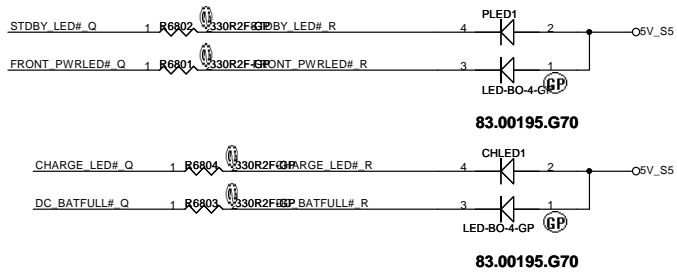
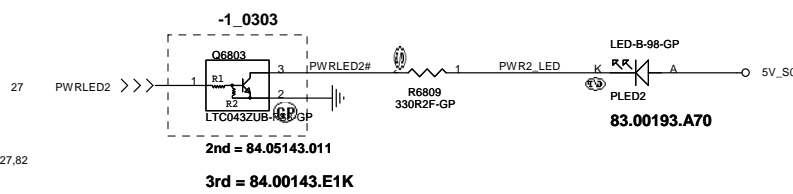
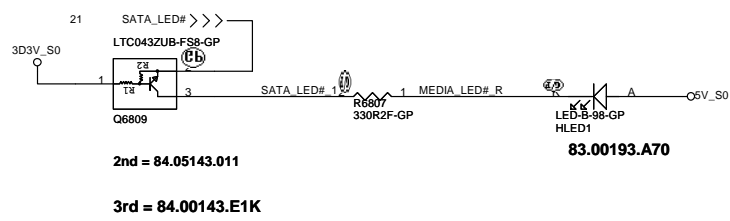
Battery LED1(CHARGE)



Caps Lock LED



SATA HDD LED



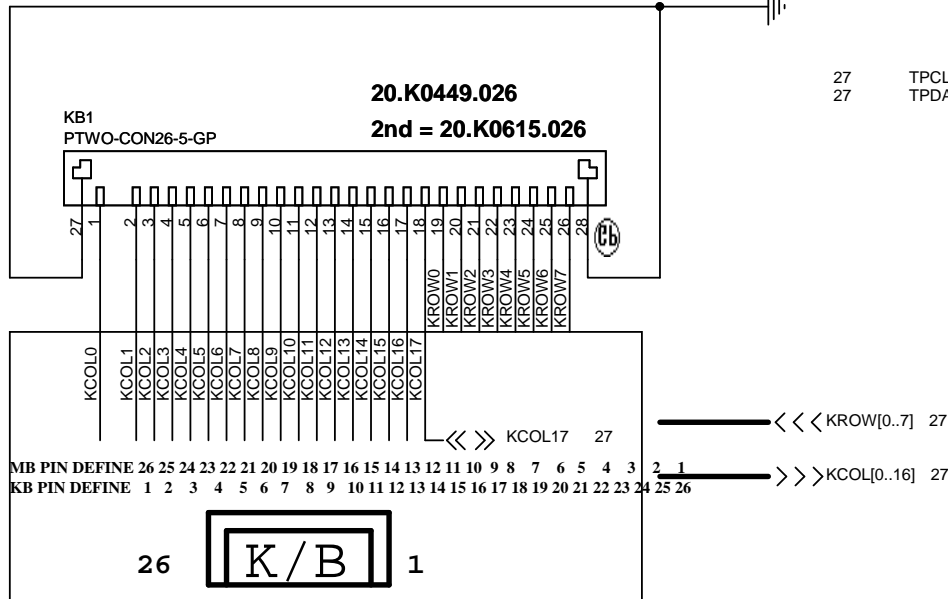
PWRLED2#	I	1	1	1	1
FRONT_PWRLED#	Q	1	1	1	1
CHARGE_LED#	Q	1	1	1	1
STDBY_LED#	Q	1	1	1	1
DC_BATFULL#	Q	1	1	1	1

for factory test

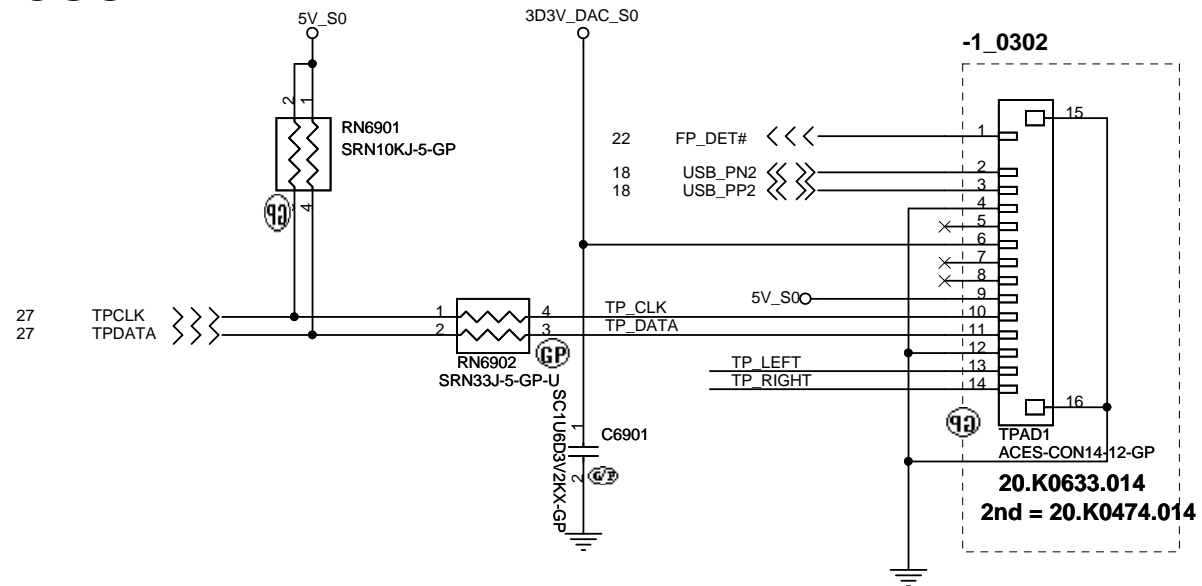
D12G	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LED Bard/Power Button	
Size Custom	Document Number BA40-HR
Date: Thursday, April 07, 2011	Sheet 68 of 109

SSID = KBC

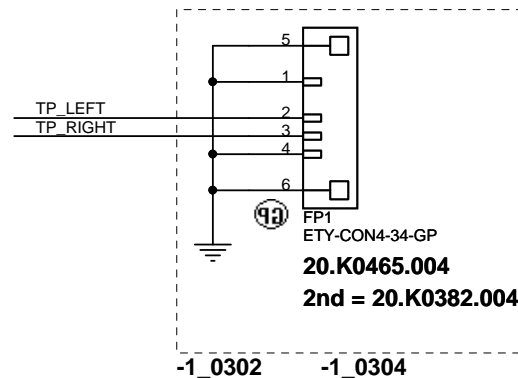
Internal KeyBoard Connector



TOUCH PAD



Rubber Dome



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size
A4

Document Number

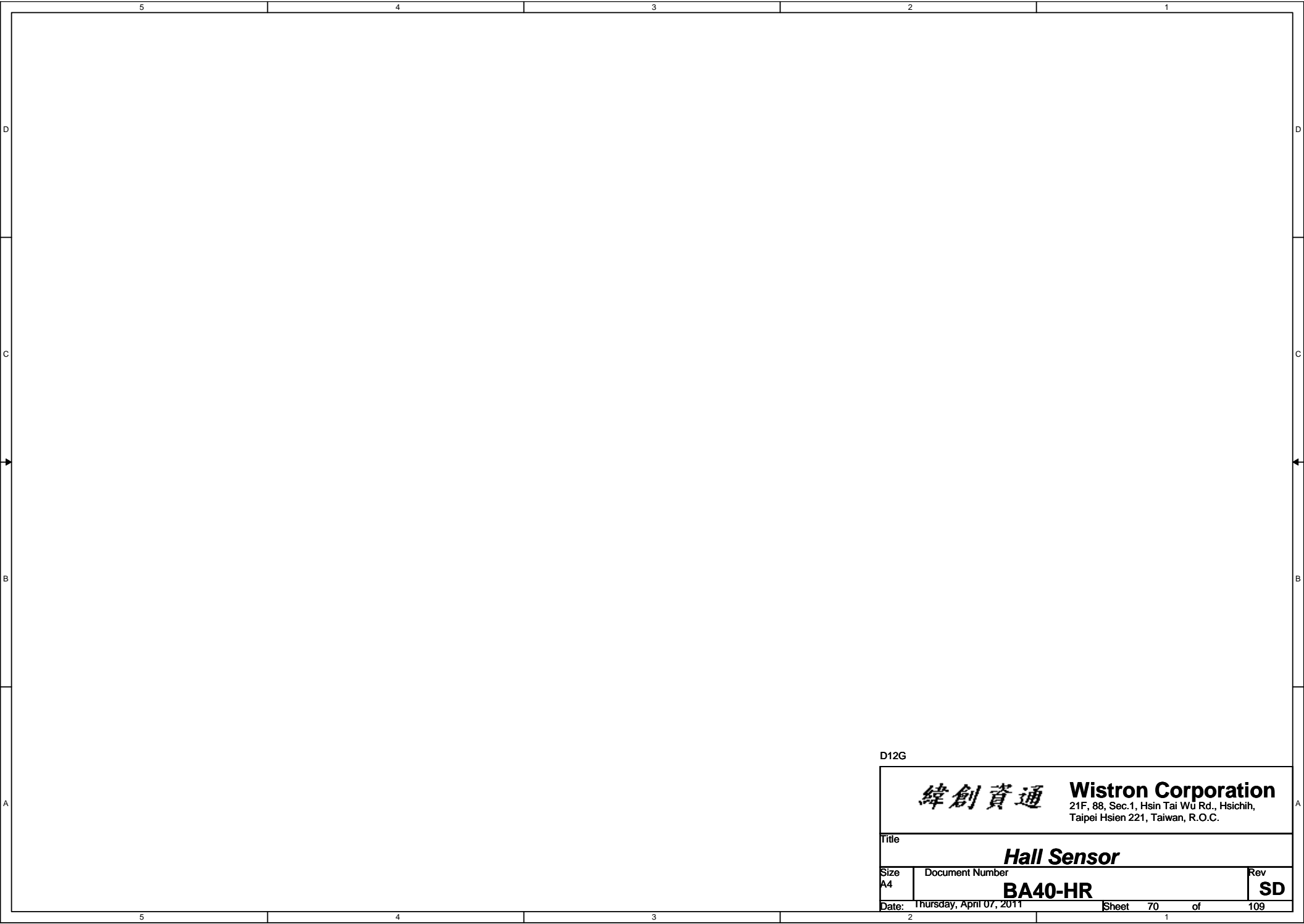
BA40-HR

Rev

SD

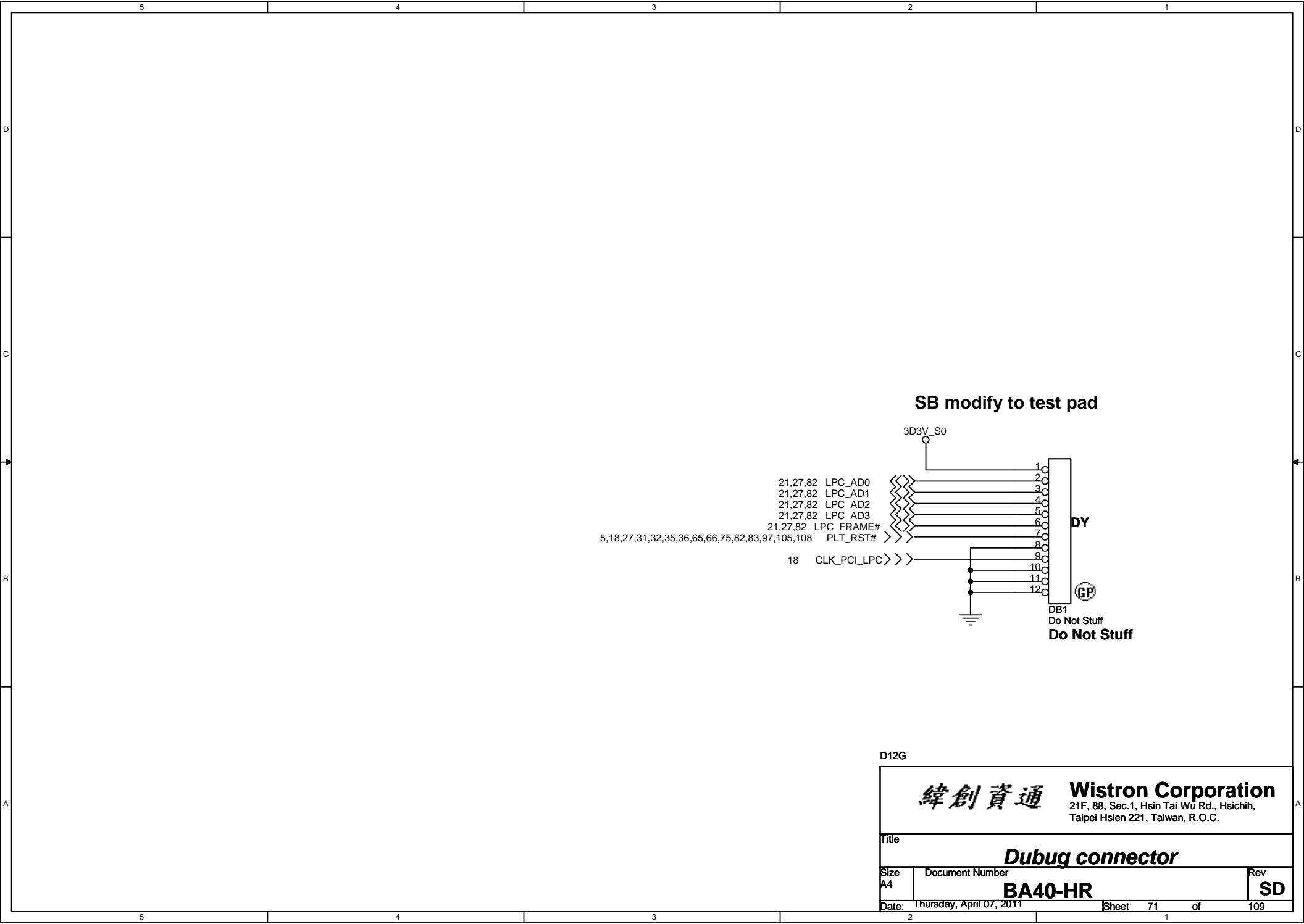
Date: Thursday, April 07, 2011

Sheet 69 of 109



D12G

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title <div>Hall Sensor</div>	
Size <div>A4</div>	Document Number <div>BA40-HR</div>
Date <div>Thursday, April 07, 2011</div>	Rev <div>SD</div>
Sheet 70 of 109	



D12G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Dubug connector		
Size	Document Number	Rev
A4	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 71 of 109

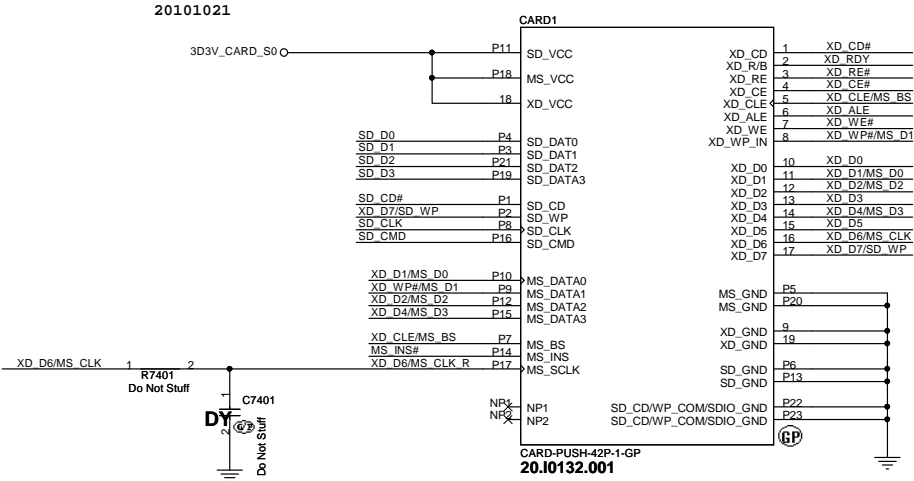
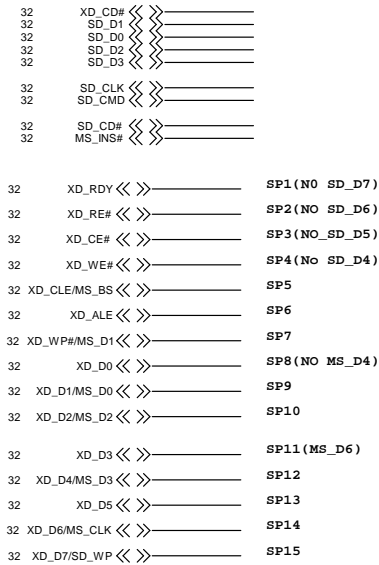
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D12G		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Reserved		
Size	Document Number	Rev
A3	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 73 of 109

SD/XD/MS Card Reader

SSID = SDIO



D12G

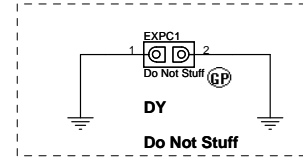
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

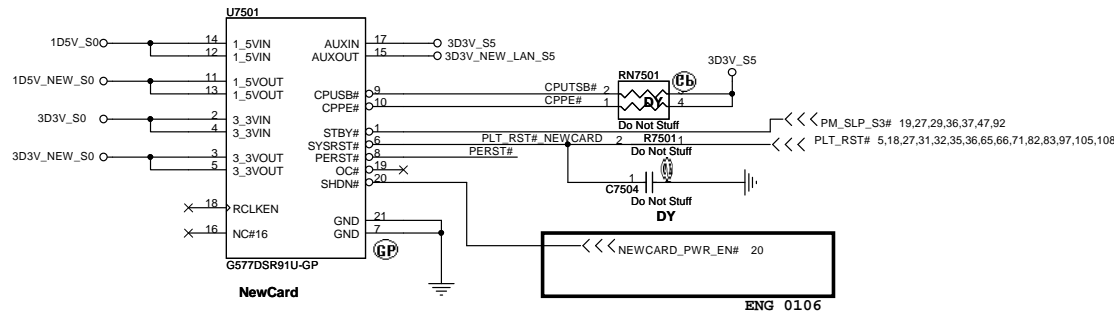
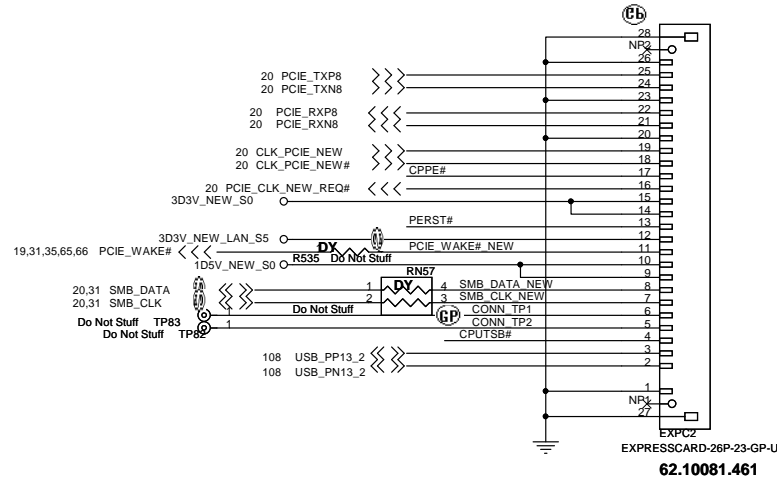
Title			CARD Reader CONN
Size	Document Number	Rev	SD
A3	BA40-HR		
Date:	Thursday, April 07, 2011	Sheet	74 of 109

SSID = ExpressCard

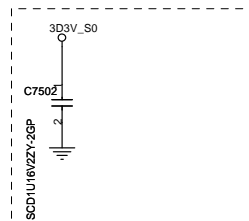
For Expresscard socket



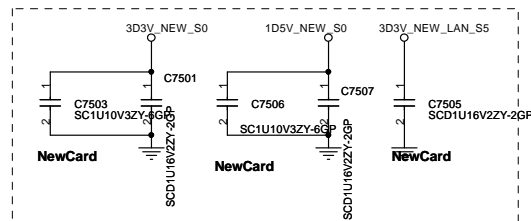
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



Place them Near to Chip



Place them Near to Connector

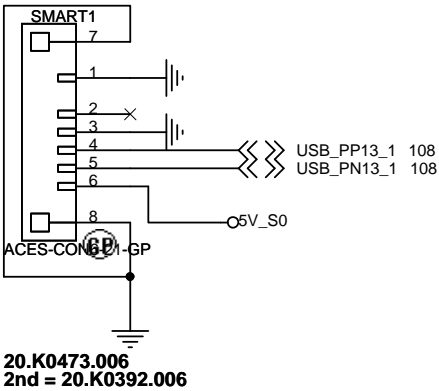


For EMI

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			New Card	
Size	Document Number	Rev		SD
A3	BA40-HR			
Date:	Thursday, April 07, 2011	Sheet	75	of 109



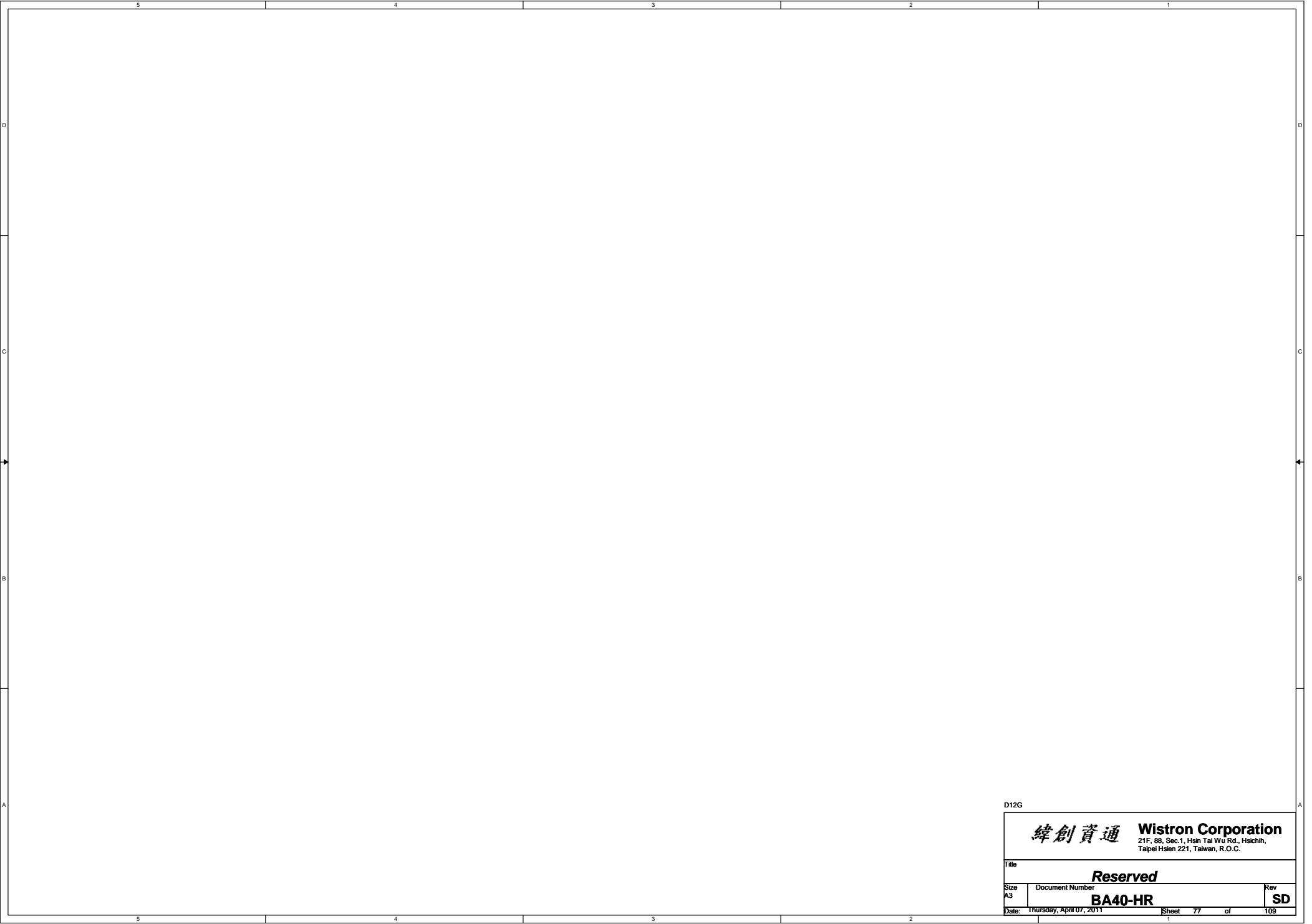
D12G

Title	
Reserved	
Size	Document Number
A4	BA40-HR
Date:	Thursday, April 07, 2011
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緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

SD



D12G		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Reserved		
Size	Document Number	Rev
A3	BA40-HR	SD
Date:	Thursday, April 07, 2011	Sheet 77 of 109

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D12G

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BA40-HR	SD
Date: Thursday, April 07, 2011		Sheet 78 of 109

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note

(1) Keep all signals are the same trace width. (included VDD, GND).

(2) No VIA under IC bottom.

D12G

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title	
Free Fall Sensor	
Size	Document Number
A4	BA40-HR
Date:	Thursday, April 07, 2011
Sheet	79 of 109
Rev	SD

(Blanking)

D12G

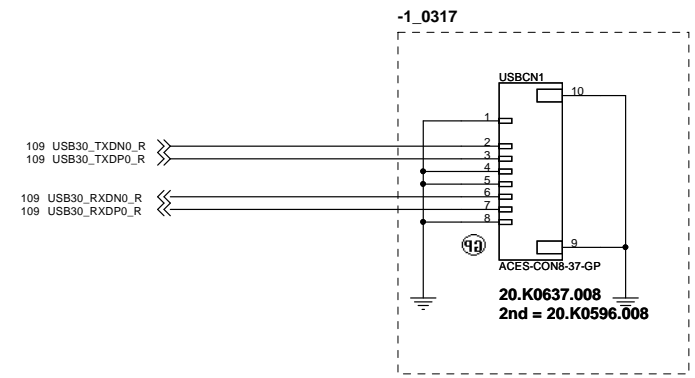
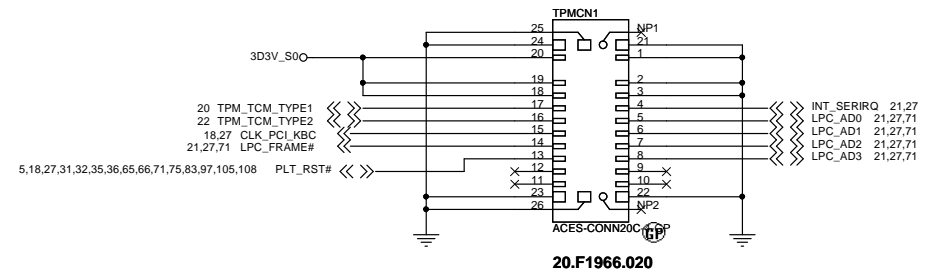
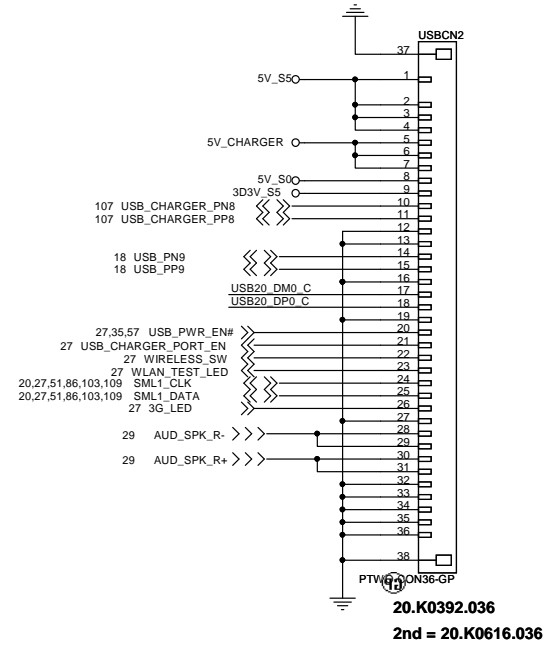
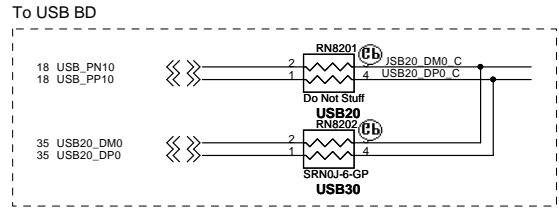
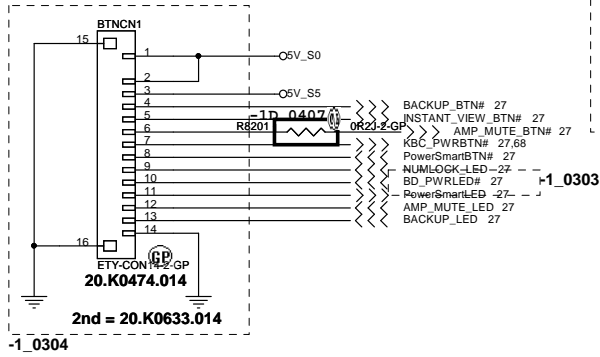
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reserved			
Size	Document Number		Rev
A4	BA40-HR		SD
Date: Thursday, April 07, 2011		Sheet 80 of 109	

(Blanking)

D12G

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BA40-HR	SD
Date: Thursday, April 07, 2011		Sheet 81 of 109

PWRCN1 FFC 異面

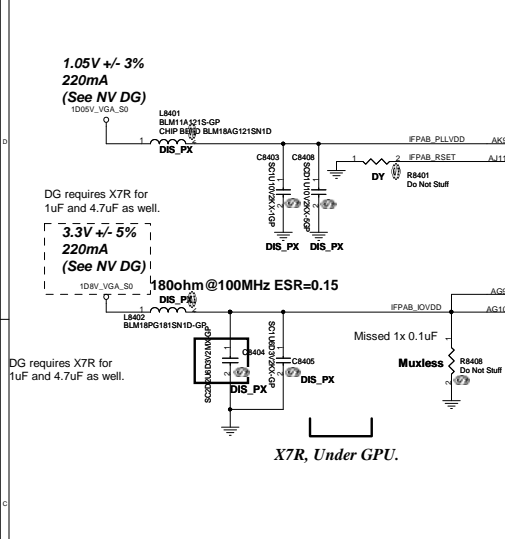


VGA1G		7 OF 16	
		IFPBn	
			IFPA_TXD0n IFPA_TXD0
			IFPA_TXD1n IFPA_TXD1
IFPBn_PLLVDD			IFPA_TXD2n IFPA_TXD2
IFPBn_RESET			IFPA_TXD3n IFPA_TXD3
			IFPA_TXCn* IFPA_TXCn
			IFPB_TXD4n IFPB_TXD4
IFPBn_OVDD			IFPB_TXD5n IFPB_TXD5
IFPBn_OVDD			IFPB_TXD6n IFPB_TXD6
			IFPB_TXD7n IFPB_TXD7
			IFPB_TXCn* IFPB_TXCn
			GRPOD

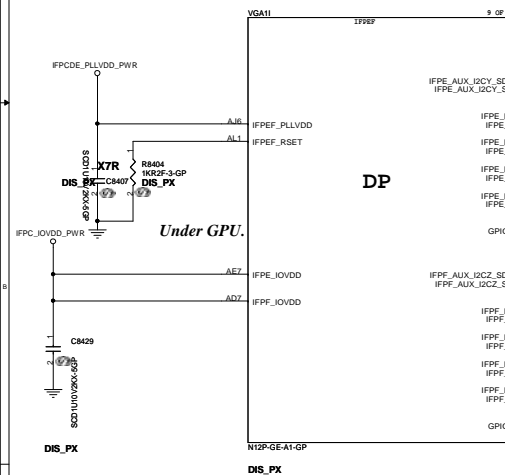
N12P-GE-A1-GP

DIS_PX

requires X7R for
4.7uF as well.

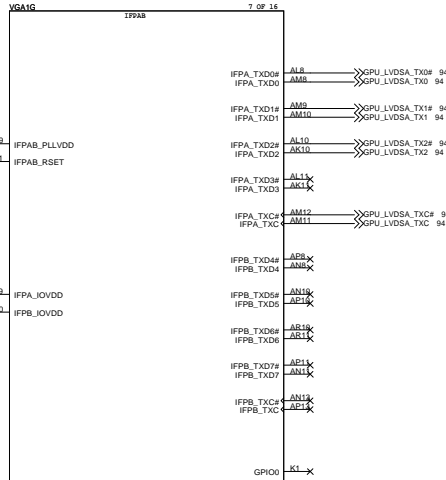


DIS_PX

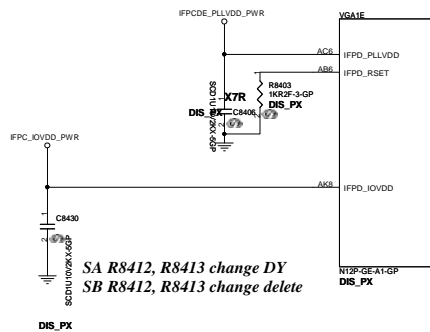


Under GPU.

DP

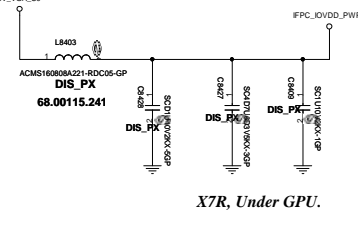


SA R8412, R8413 change DY
SB R8412, R8413 change delete

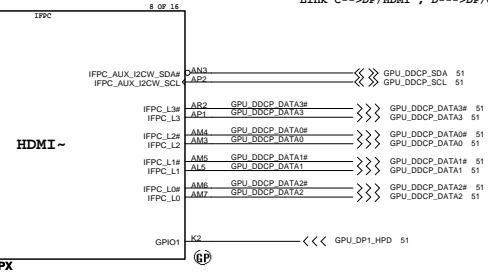
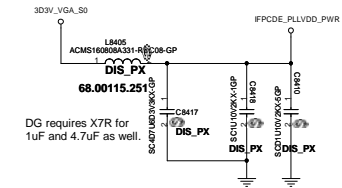


1.05V +/- 3%
285mA
(See NV DG) 220ohm@100MHz ESR=0.05
1D05V_VGA_S0

X7R, Under GPU.

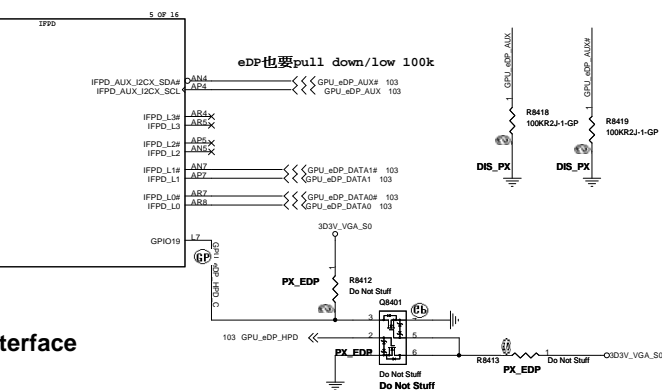


3.3V +/- 5%
440mA (220mA each, max 2 links)
(See NV DG) 300ohm@100MHz ESR=0.25



Link C-->DP/HDMI ; D--->DP/eDP ; E--->

eDP也要pull down/low 100k

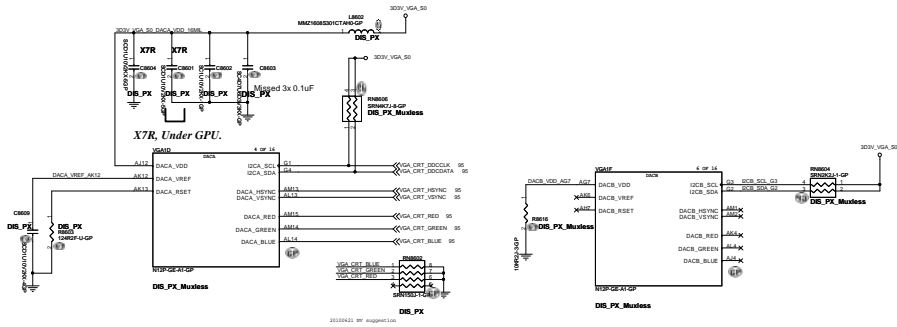


DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

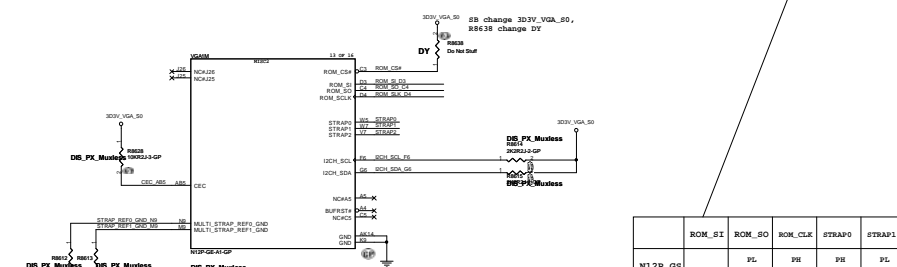
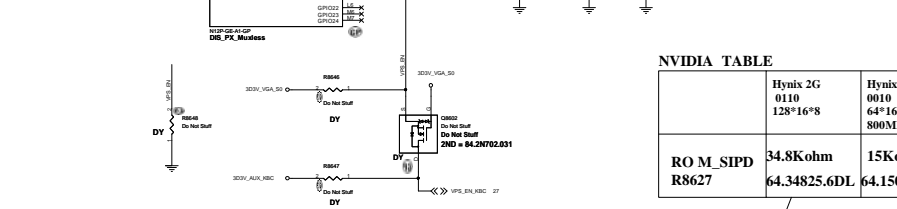
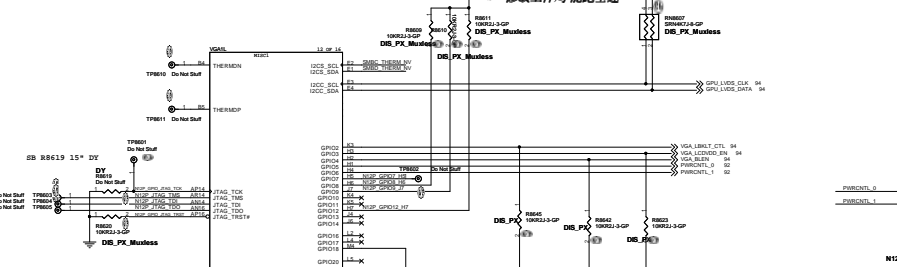
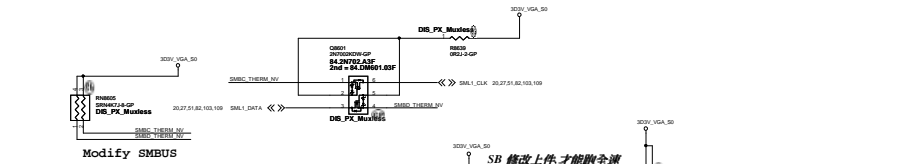


300ohm@100MHz ESR=0.25ohm

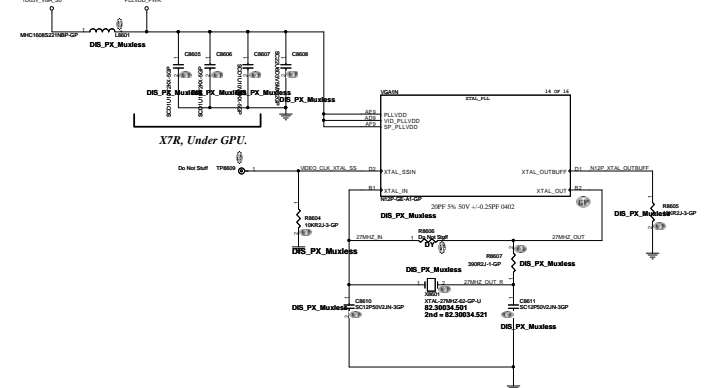
3.3V +/- 3%
120mA
(See NV DG)



VGA Thermal sensor P2800



1.05V +/- 3%
150mA
(See NV DG)



N12P-GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D5	VGA_CORE_PWR
L	L	L	0.825V
H	L	L	0.9V
L	H	H	0.975V
H	H	H	1V

default boot voltage table

Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
64M16 DCR3	Hynix	2x2	H5TG1640DFR-11C	900/900
	Samsung	2x3	K6W1G1640E-HC11	900
	Samsung	TEC	K6W1G1640G-BC11	900/900
	Hynix		H5TG1640DFR-12C	900
	Samsung		H5TG1640DFR-12C	900
	Samsung		K6W1G1640E-HC12	900

NVIDIA TABLE

	Hynix 2G 0110 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

	ROM_S1	ROM_S0	ROM_CLK	STRAP0	STRAP1	STRAP2
N12P-GS	PL 10K ohm	PH 15K ohm	PH 45K ohm	35K ohm	25K ohm	PL
N12P-GV	PH 10K ohm	PH 5K ohm	PH 45K ohm	35K ohm	5K ohm	PL

TABLE

NVIDIA	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

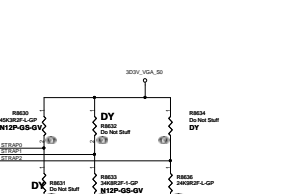
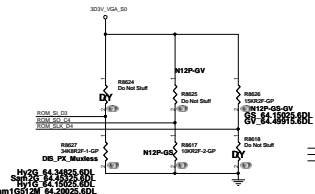
N12P-GS
USE I111 (45K)

N12P-GV

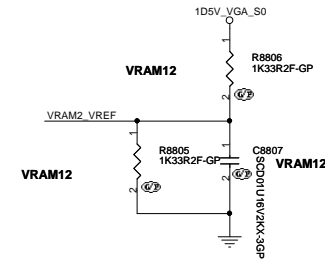
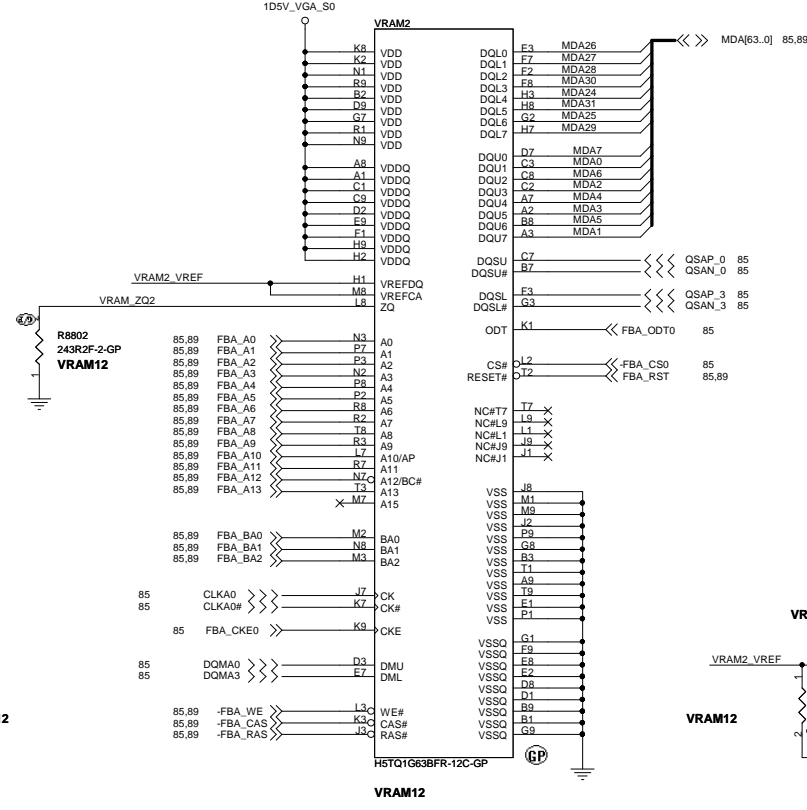
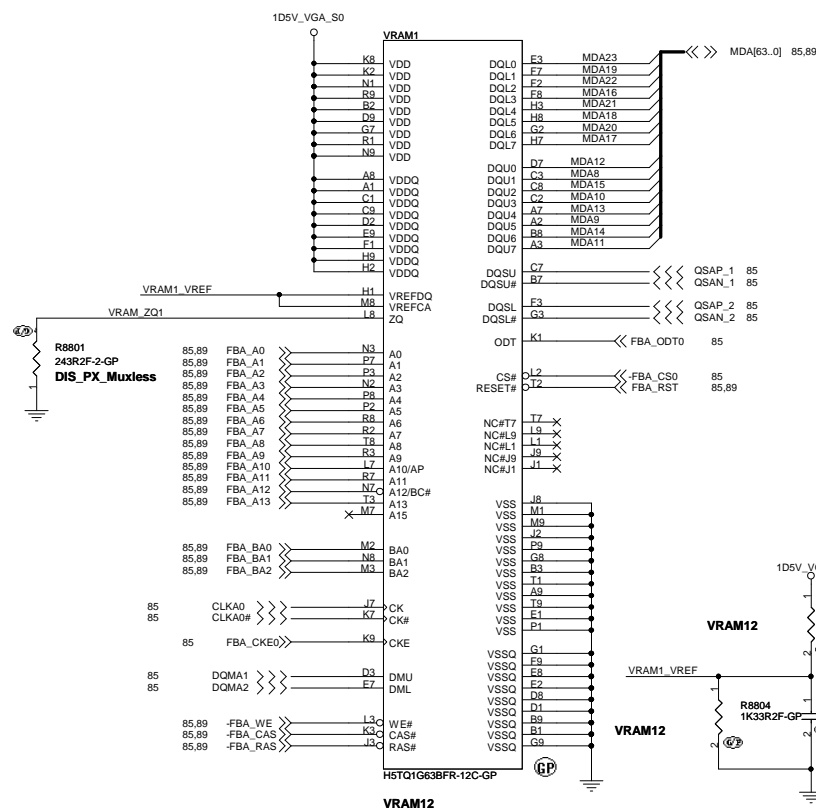
N11P-GE
Pull Low

N11P-GS
Pull Low

N12P-GE







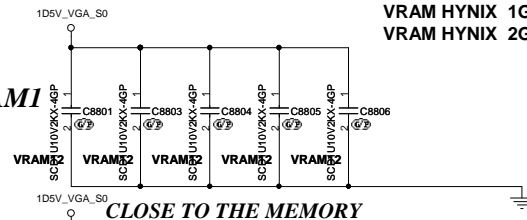
Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2GX8
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

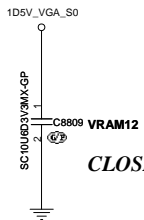
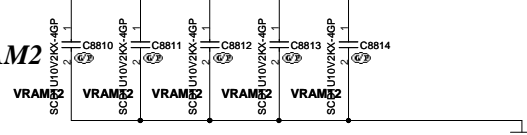
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

FOR VRAM1

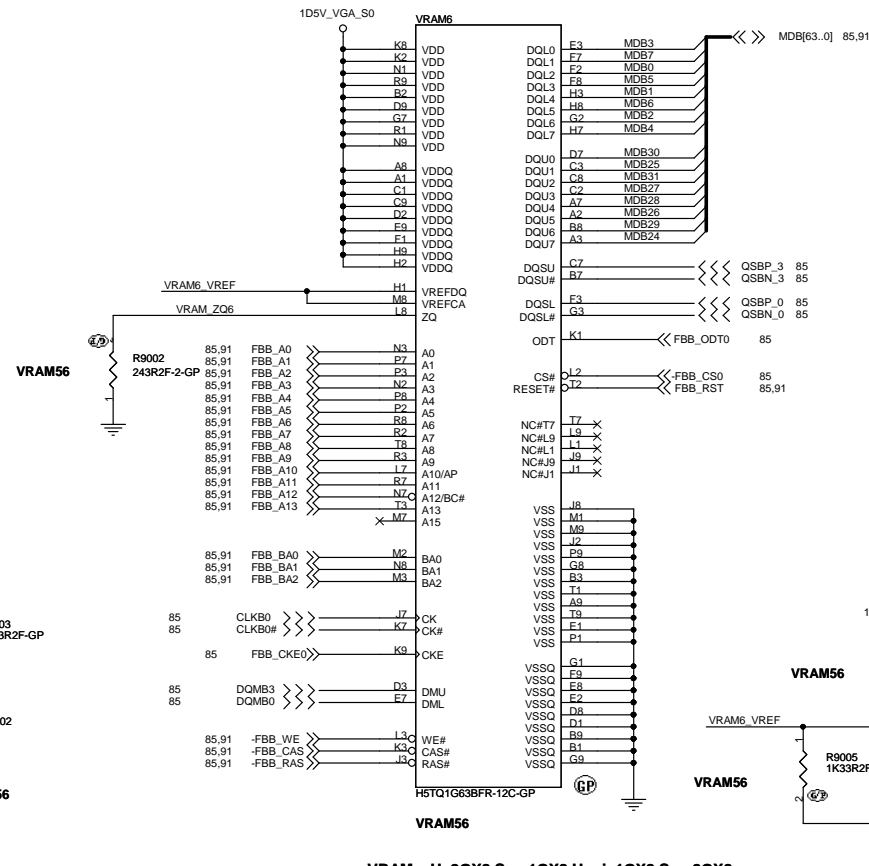


CLOSE TO THE MEMORY

FOR VRAM2

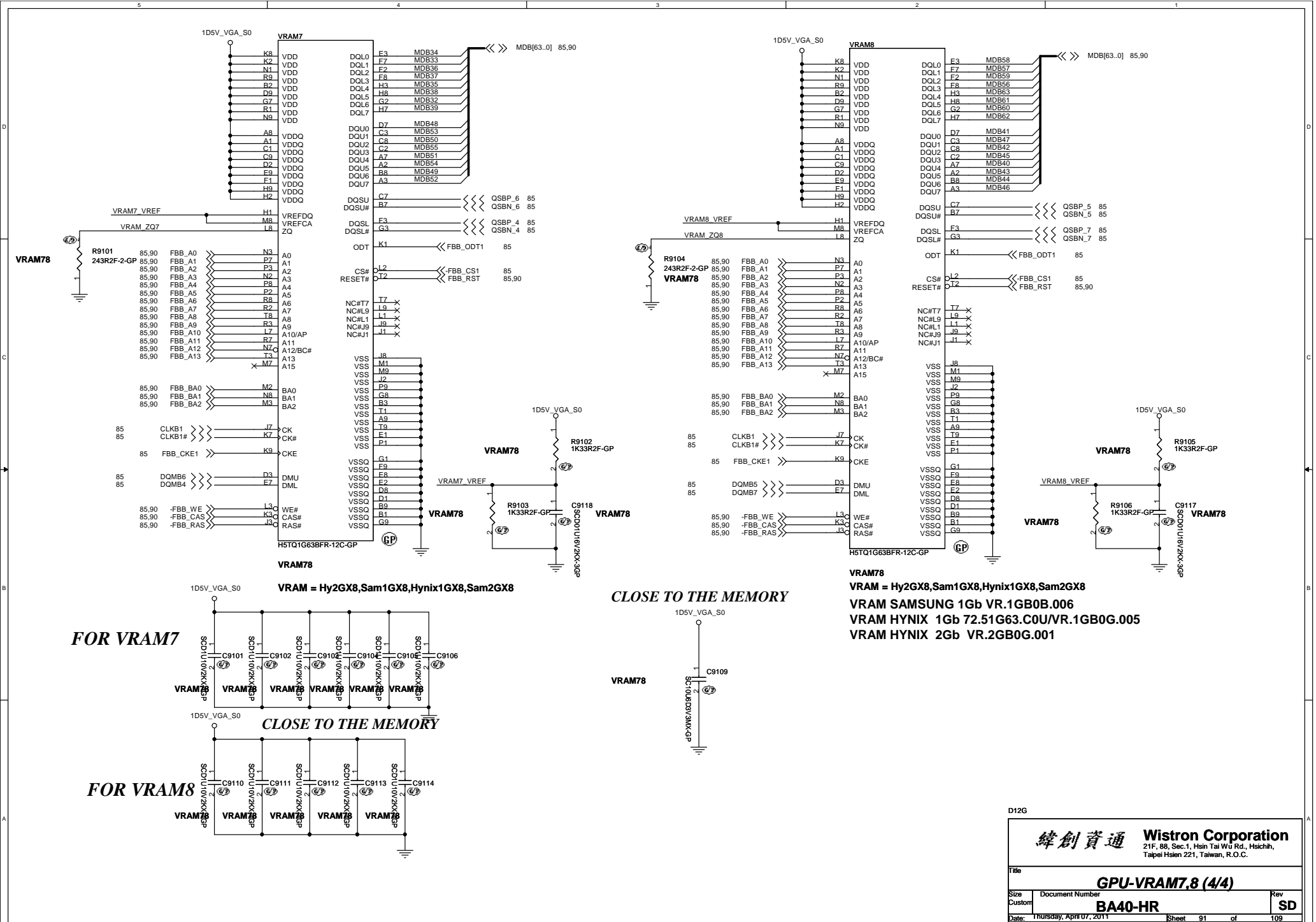


CLOSE TO THE MEMORY

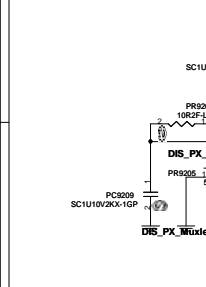
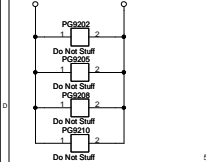


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

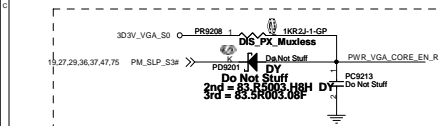
 緯創資通		Wistron Corporation 2/F, 88, Sec. 1, Hsien Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM5.6 (3/4)			
Size	Document Number		Rev
Custom	BA40-HR		SD
Date:	Thursday, April 07, 2011	Sheet	90 of 109



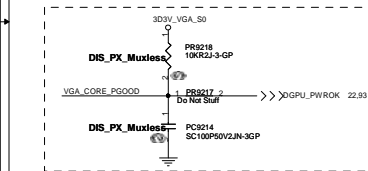
DCBATOUT PWR_DCBATOUT_VGA_CORE



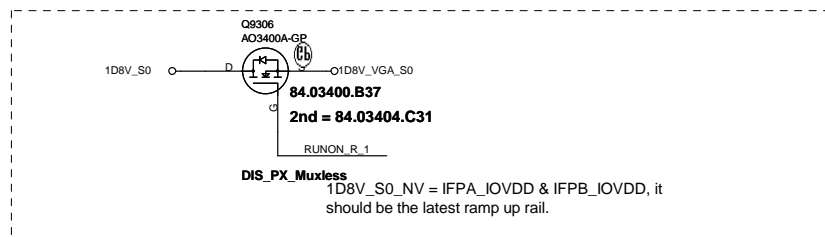
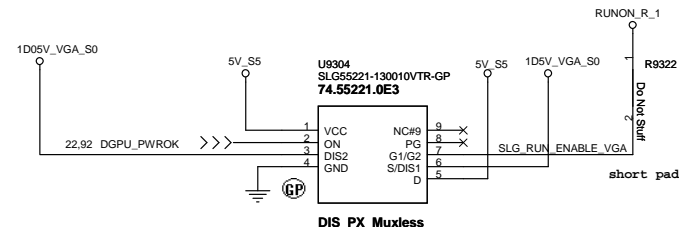
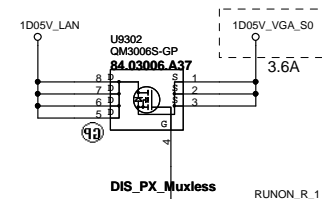
RT8208A:74.08208.073



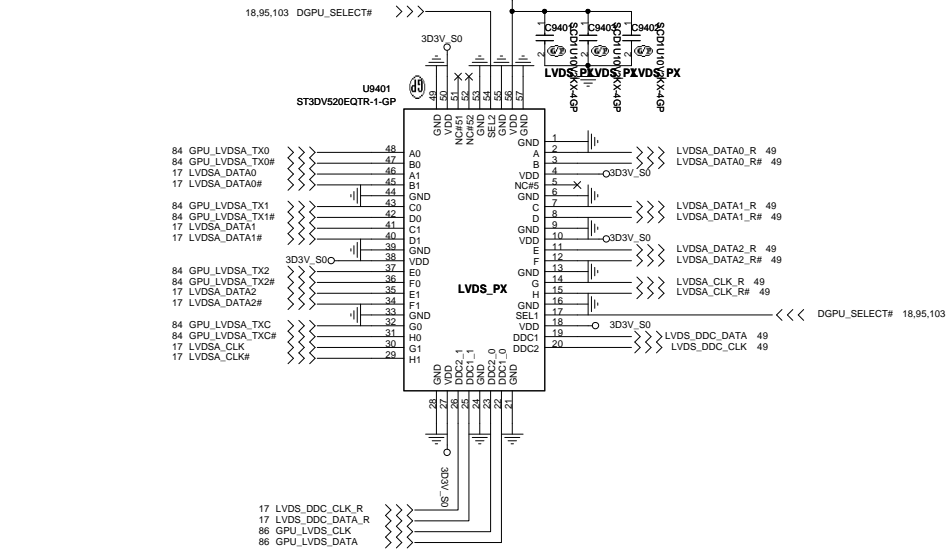
Do Not Stuff
2nd = 83.500000H
3rd = 83.500000H



1.05V to 1.05V_VGA_S0 Transfer



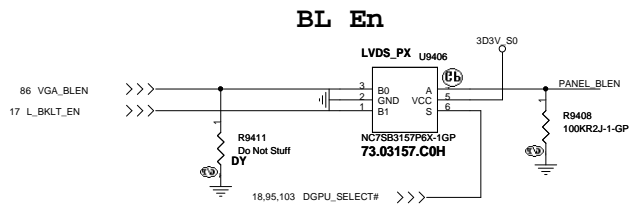
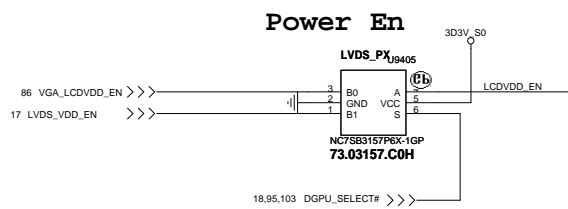
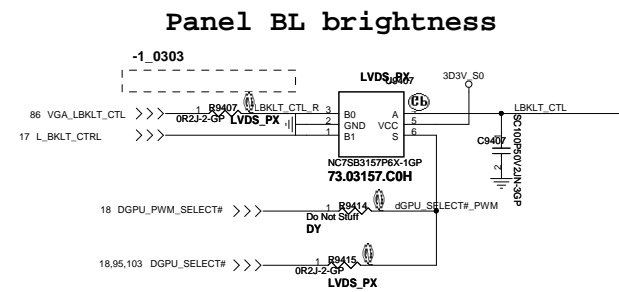
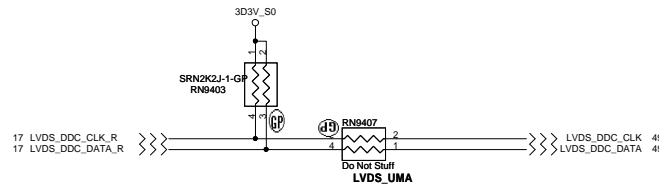
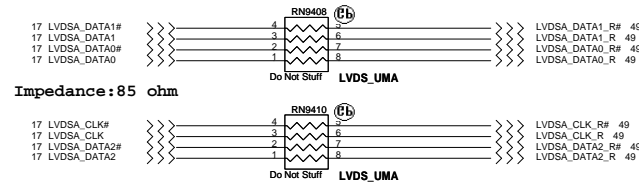
LVDS



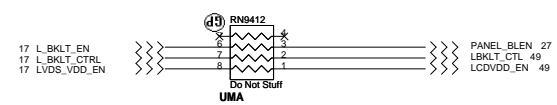
SEL->L(X=nX0),H(X=nX1)

SEL1 Control A~H

SEL2 Control DDC1,DDC2



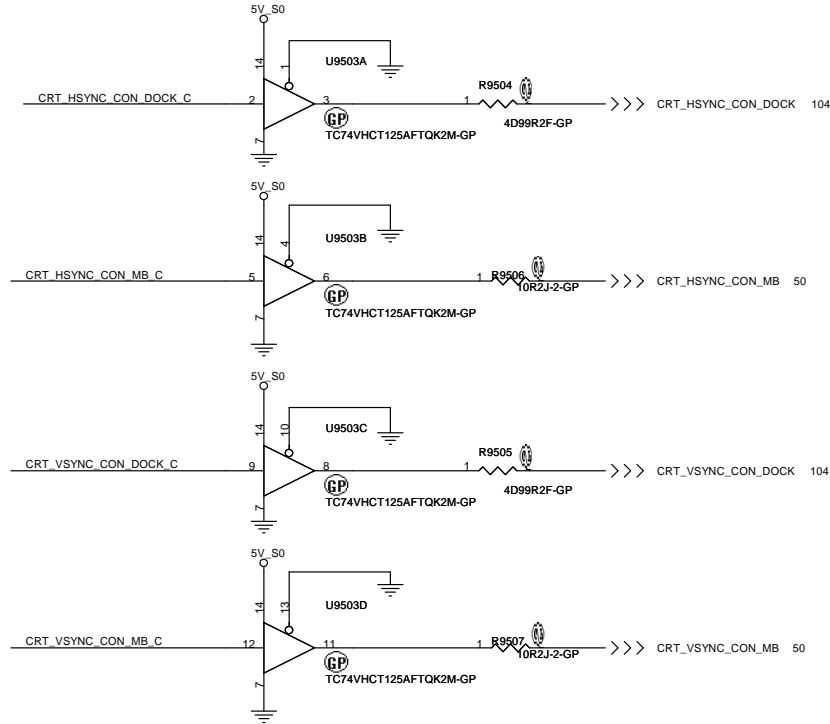
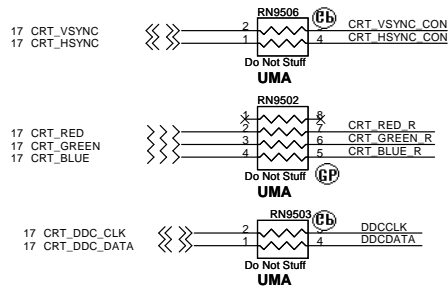
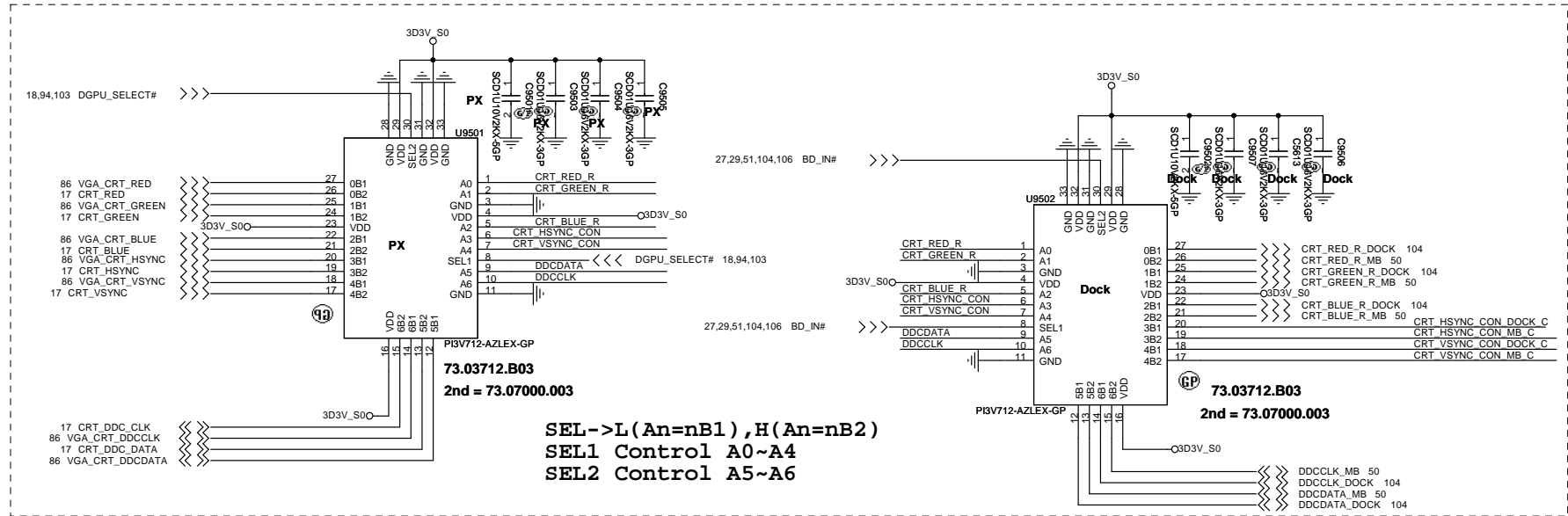
Panel BL brightness/Power En/BL En



CRT DDCDATA & DDCCLK

VDD :

Recommend to use 6 caps ($0.1\mu + 5 \times 10nF$) close to our chips



D12G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT_Switch

Size
A3

Document Number

Huron River

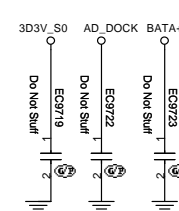
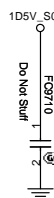
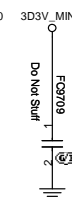
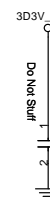
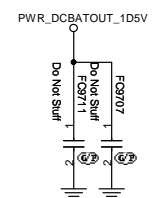
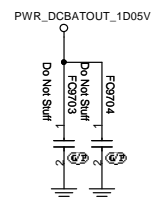
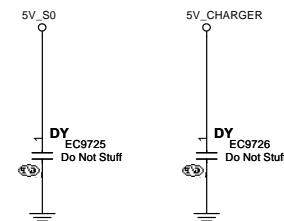
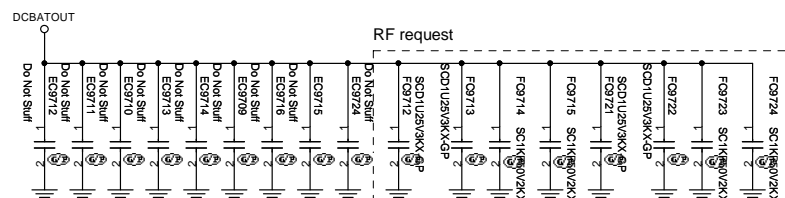
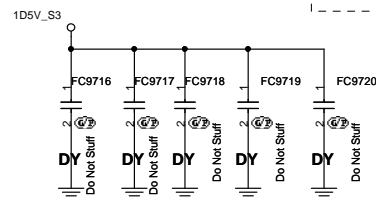
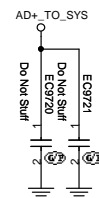
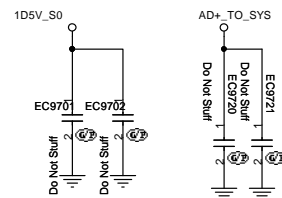
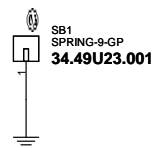
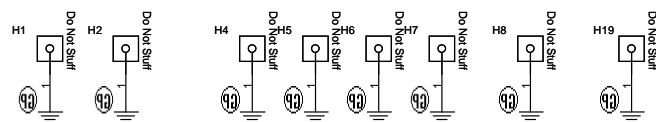
Rev
SD

Date: Thursday, April 07, 2011

Sheet 95

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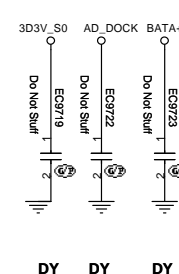
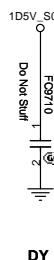
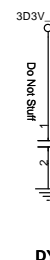
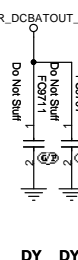
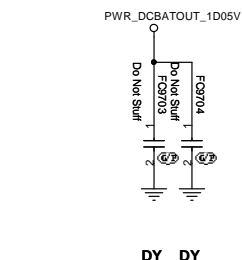
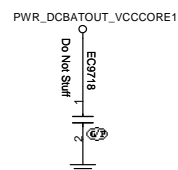
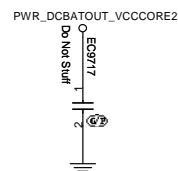
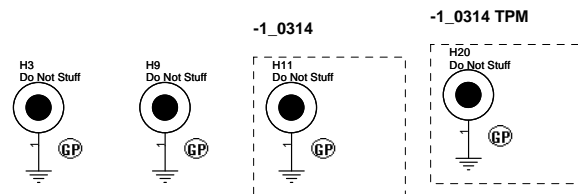
SSID = SDIO



Check test point

3D3V_S0	1	⊗	AFTP1
3D3V_AUX_S0	1	⊗	AFTP7
3D3V_S5	1	⊗	AFTP8
5V_S5	1	⊗	AFTP9
PM_PWRBTN# <<<	1	⊗	AFTP10
4_CUPWWRGD >>>	1	⊗	AFTP11
S5_ENABLE <<<	1	⊗	AFTP12
3_PLT_RST# >>>	1	⊗	AFTP13

Test Point放在Dimm Door打開可量測處



DY DY

DY DY

DY

OCBATOUT

RF request

DY DY DY DY DY DY DY DY DY

DY DY

DY DY

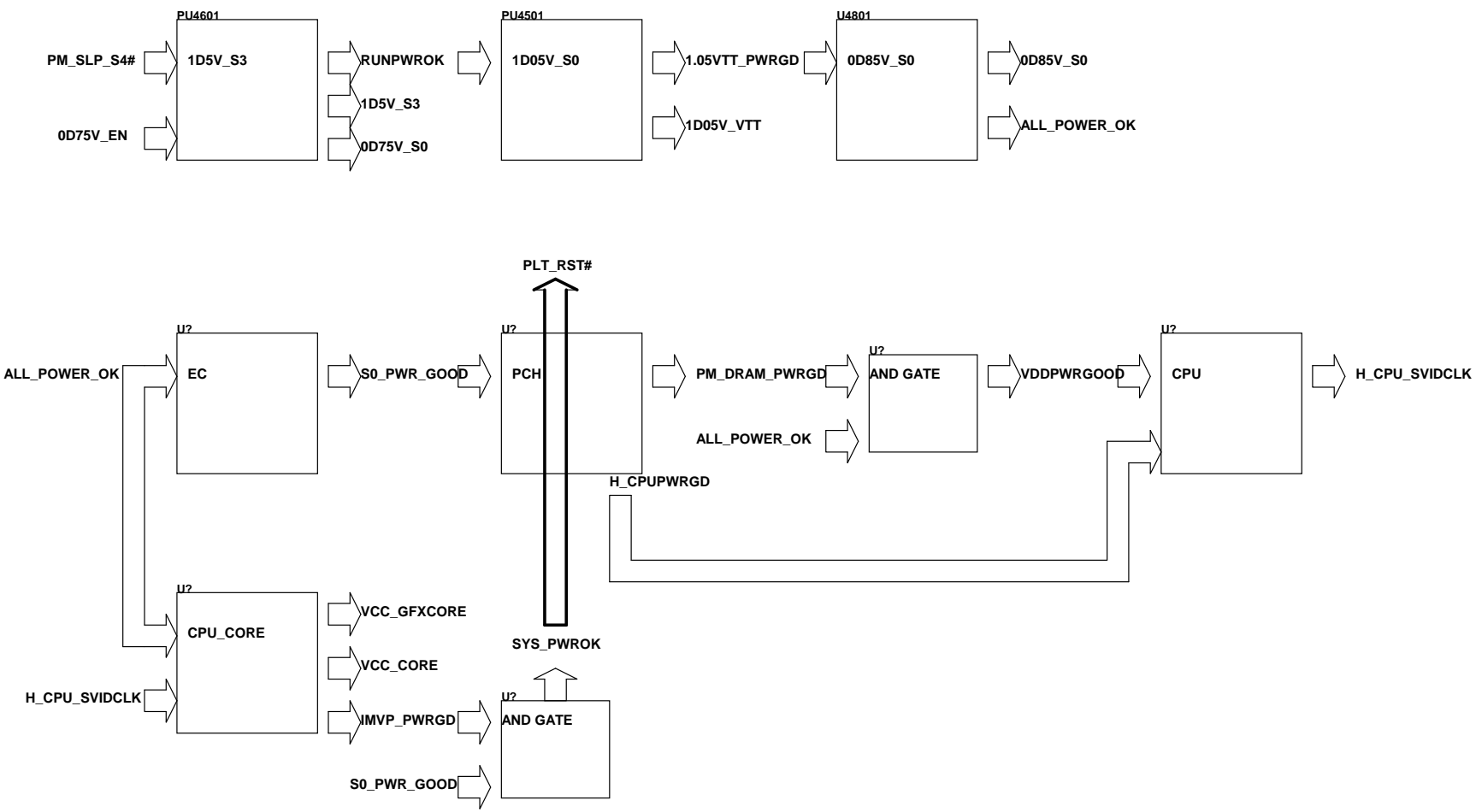
DY

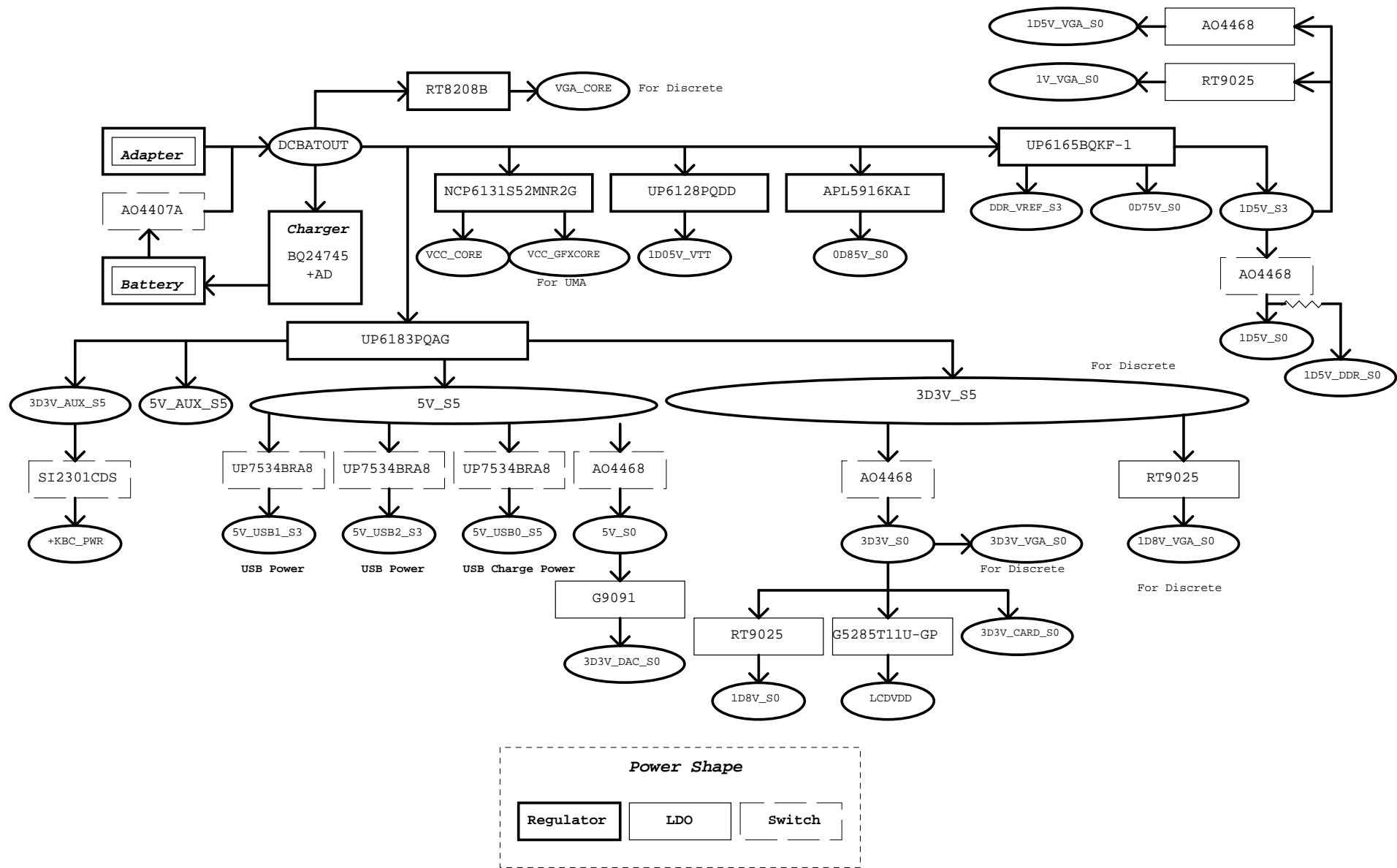
DY

DY

DY DY DY

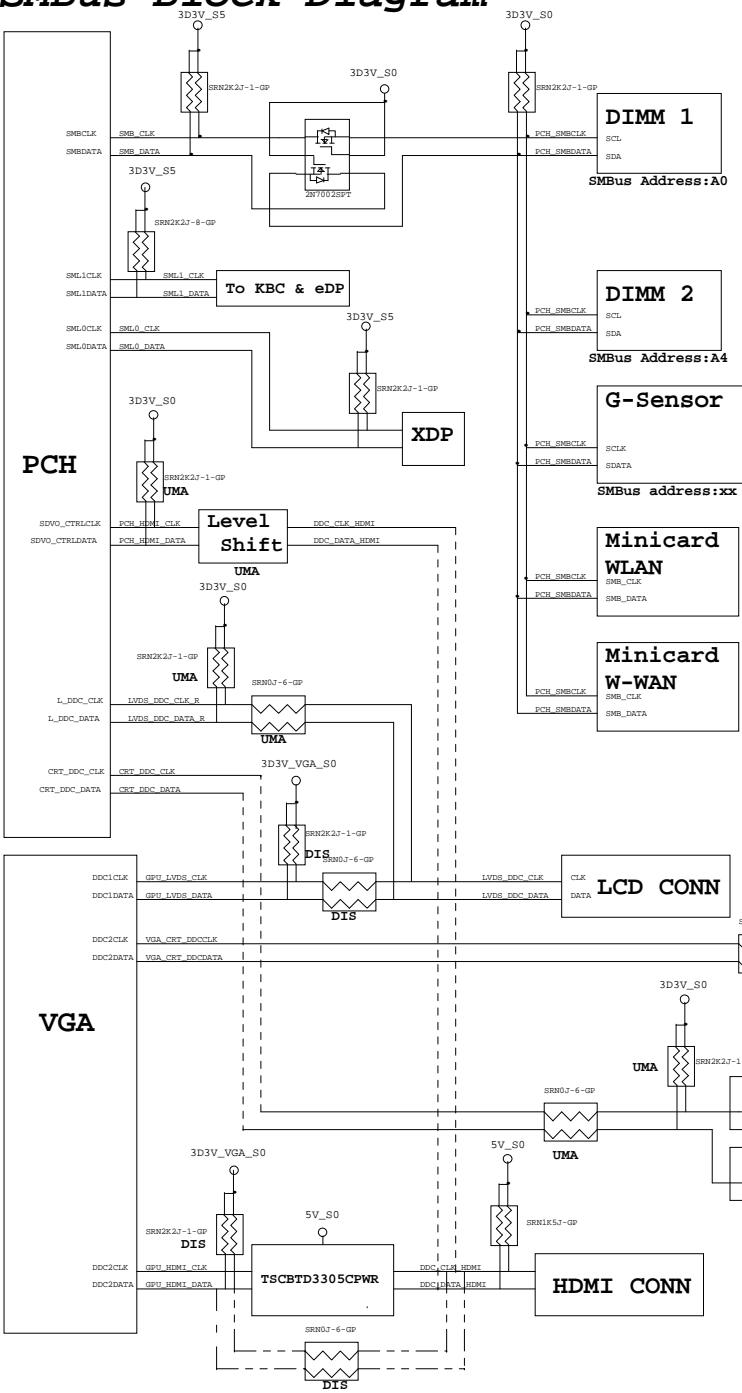
Power Sequence



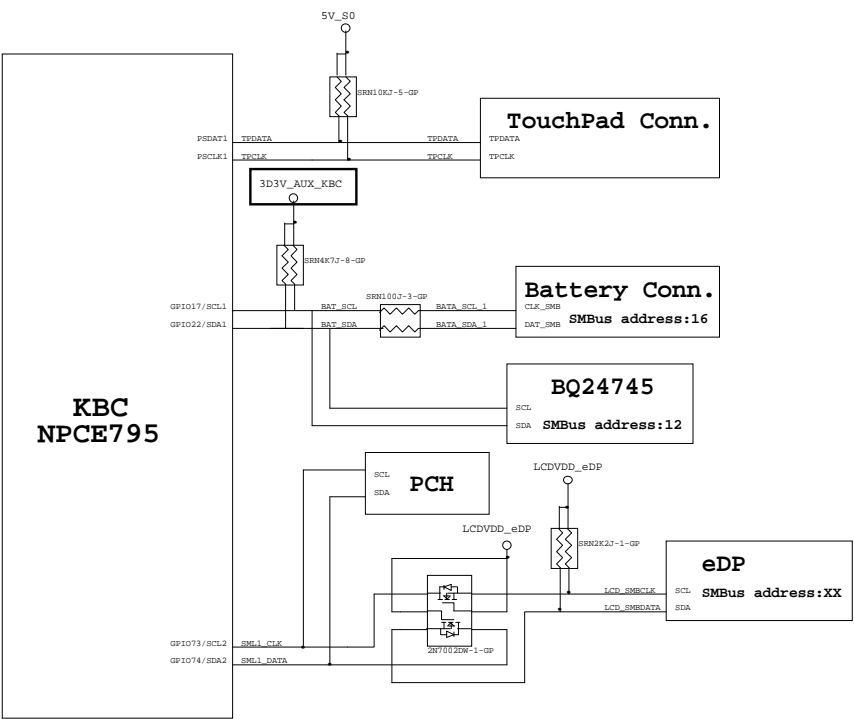


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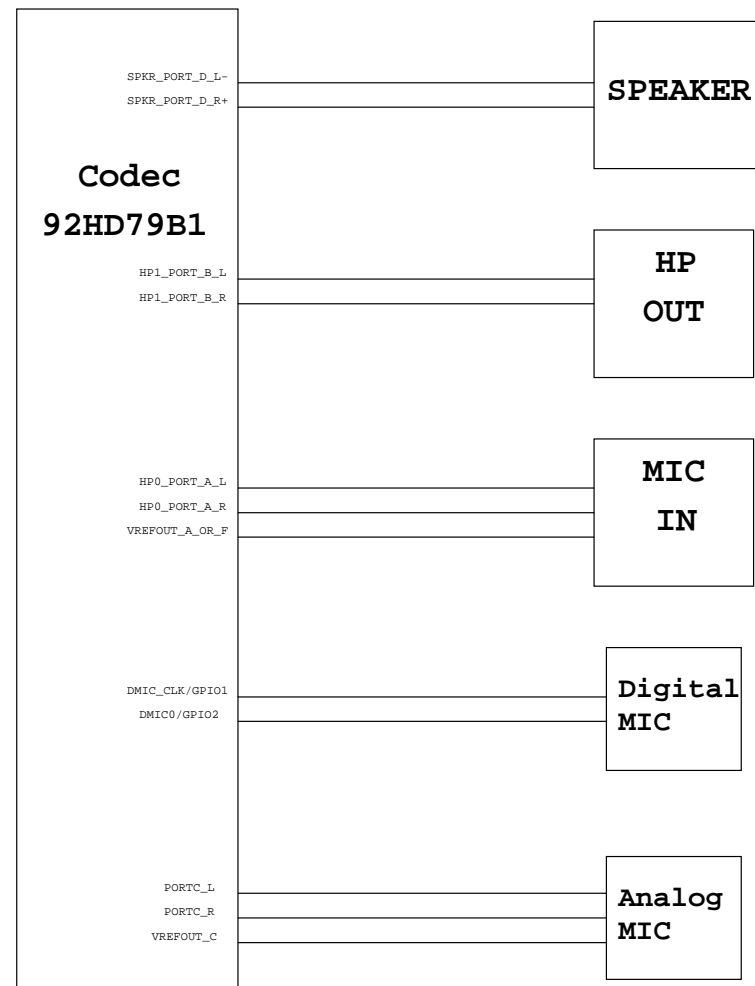
PCH SMBus Block Diagram

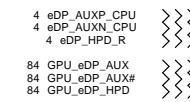
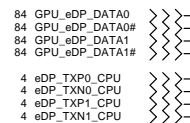
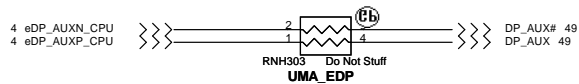
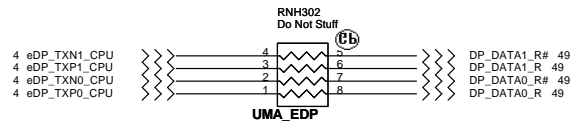


KBC SMBus Block Diagram

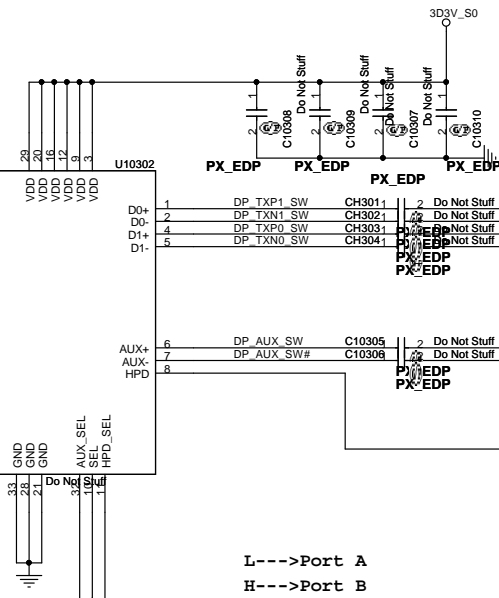


Audio Block Diagram

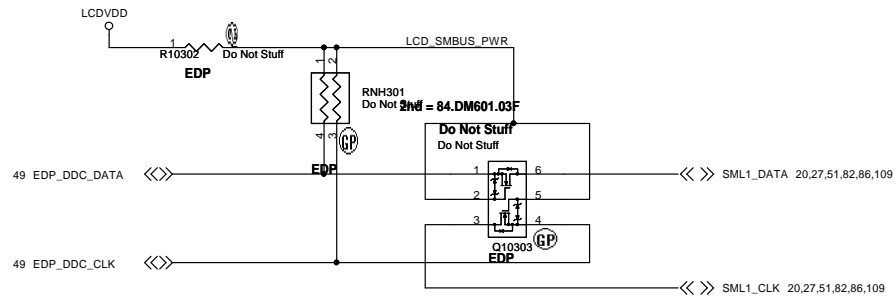


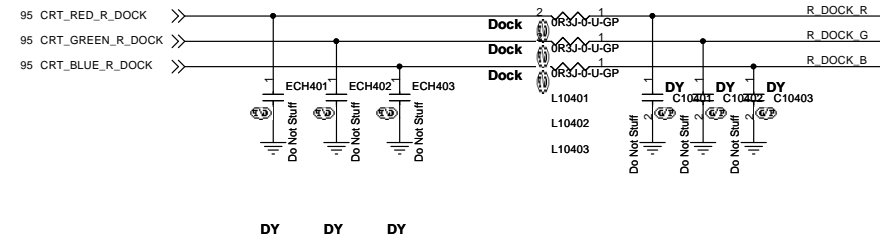
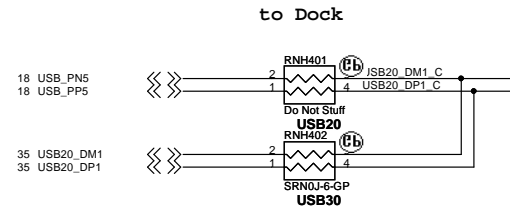
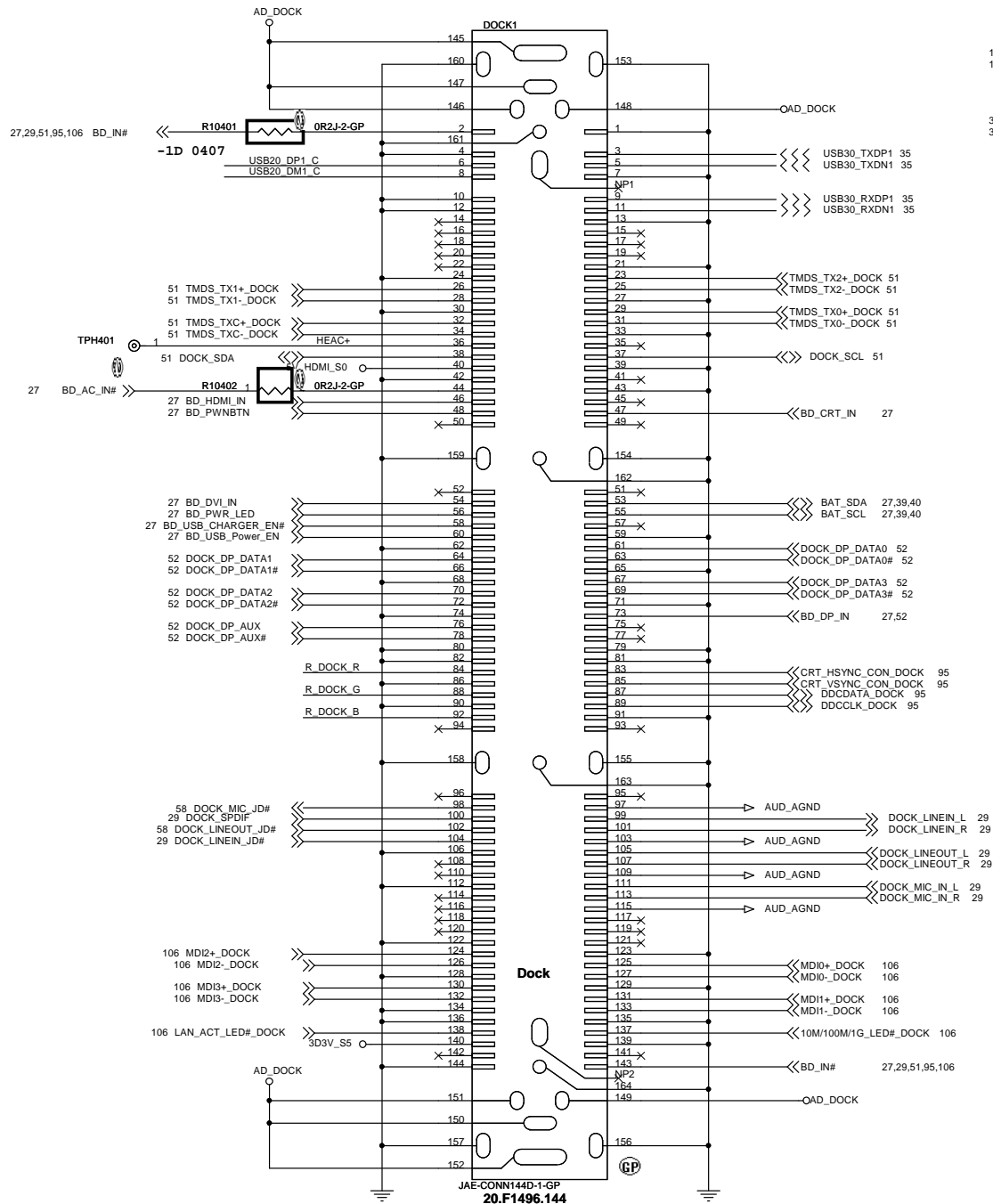


18,94,95 DGPU_SELECT#



L--->Port A
H--->Port B

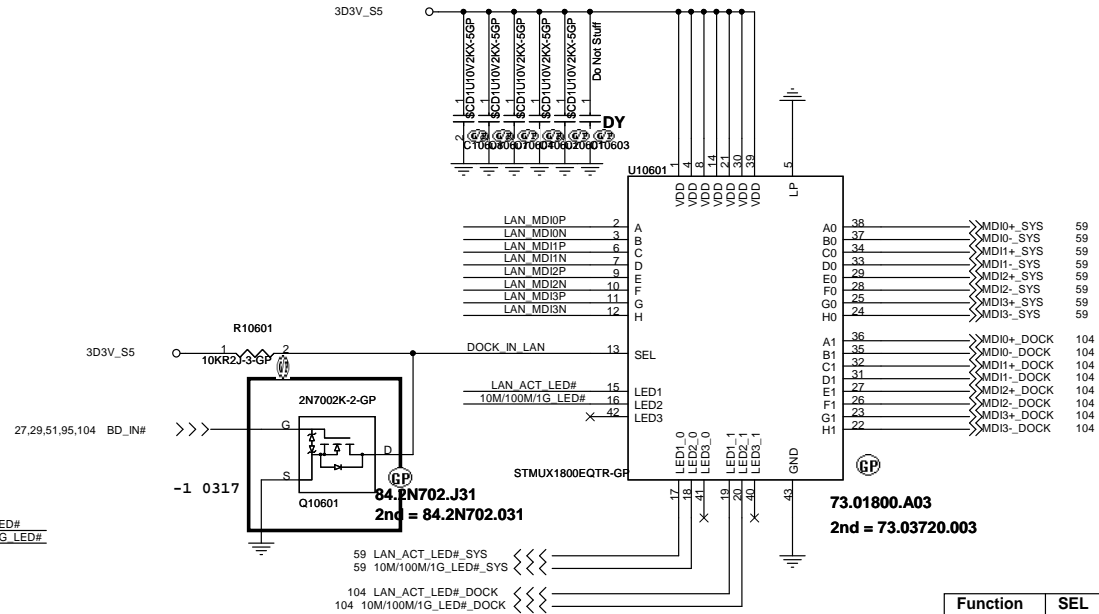
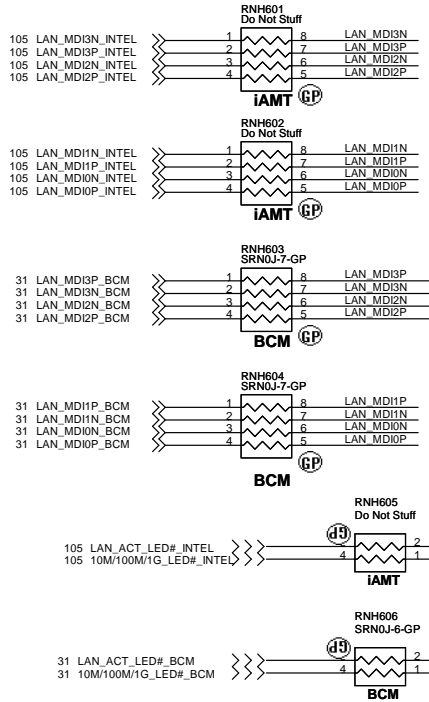




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Title BOTTOM DOCKING	
Size A3	Document Number BA40-HR
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LAN switch

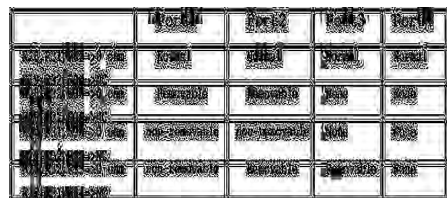
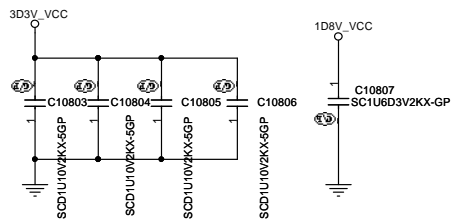


Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

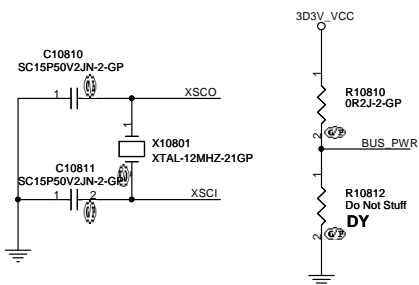
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Taipei Hsien 221, Taiwan, R.O.C.

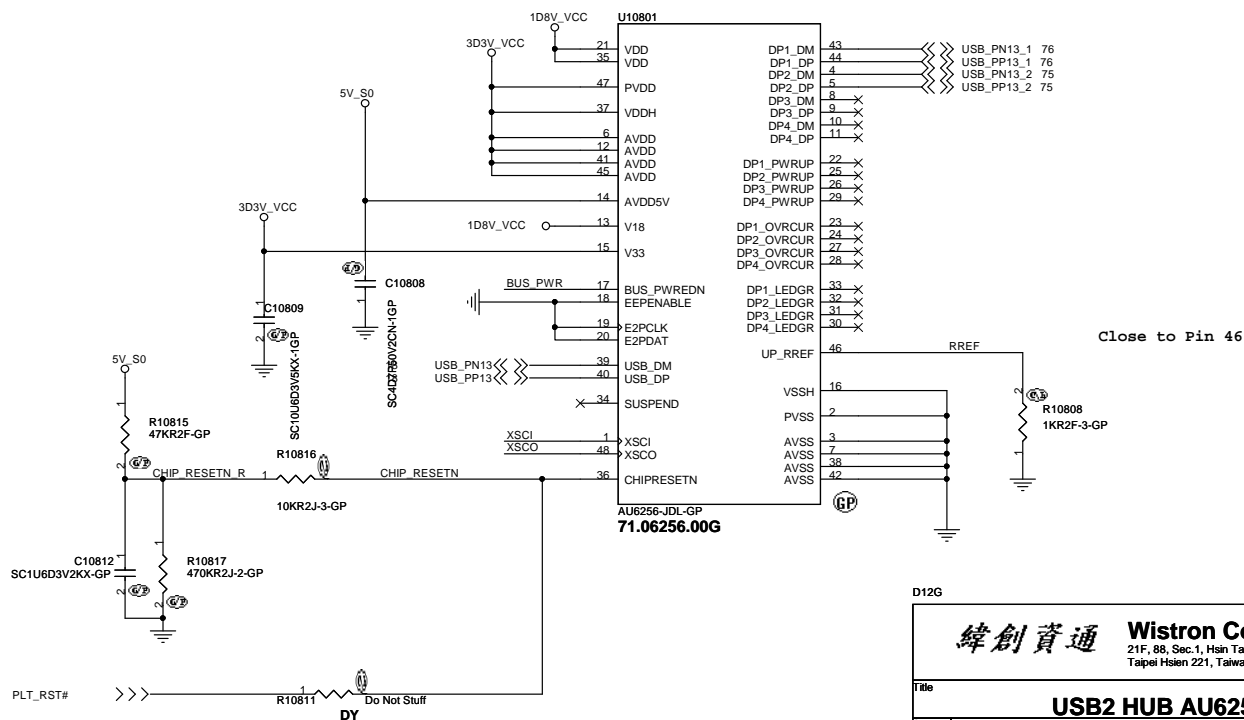
Title			LAN SWITCH		
Size	Document Number				Rev
A3	BAD50-HR				SD
Date:	Thursday, April 07, 2011	Sheet	106	of	109



EEPENABLE
0 : Use Internal Rom
1 : Use External Rom



5,18,27,31,32,35,36,65,66,71,75,82,83,97,105 PLT_RST#

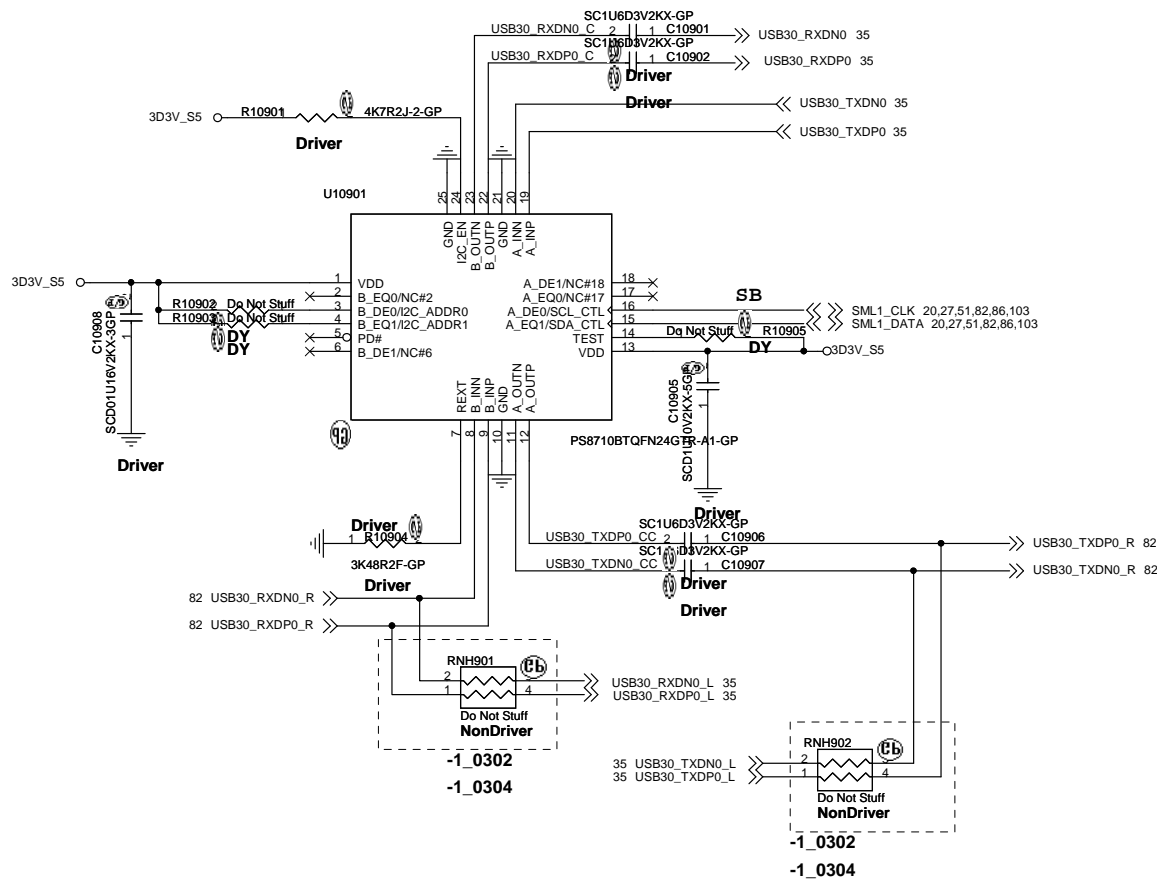


D12G

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Title		
USB2 HUB AU6256		
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I2C mode
To USB BD



D12G